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CF Card

Table of Contents

Compact Flash Card

1. Description

1.1 Product Overview

CompactFlash™ based on flash memory controller technology. This card complies with **CompactFlash™** specification, it is suitable for the usage of data storage memory for PC or other electric equipment and digital still camera. This card is equipped with NAND flash memory. By using this card it is possible to operate stability for the system that have **CompactFlash™** slots.

- **Application Fields;**
  - Industrial PC and Thin Client
  - Game and Telecommunication Machine
  - Ticketing, Examining, testing machine
  - Army, Health and Production Equipment and Machine

1.2 Features

- Compact Flash™ specification: PCMCIA ver.2.1 and PC Card ATA ver.2.01 compatible 50pin SMT connector and type I (3.3mm).
- 3.3V/5V single power supply operation.
- Internal self-diagnostic program operates at VCC power on.
- 3 variations of access mode:
  - Memory Card Mode, I/O Card Mode, True-IDE Mode.
- High reliability based on internal ECC (Error Correcting Code) Function.
- Data reliability is 1 error in 10^{14} bits read.
- Support PIO Mode4 and Multi-word DMA mode2.
- Operation Temperature range: -25 to 65 ℃.
- Power Consumption (3.3V/ 5.0V).
- High Performance:
- Have hardware (switch) to execute write protect function,

  Notes: The performance will depend on different platform with different test result.

1.3 System Requirement

- The Host system which is connected to Disk On Module should meet system requirements at minimum;

1.3.1 Power Requirement

- Voltage: DC +3.3V ± 5% or DC +5.0V ± 10%

1.3.2 Operating System

- Windows XP/7/8/8.1
- Linux
- DOS
- WinXP Embedded
- WinCE

1.3.3 Interface

- IDE (ATA) Standard Interface

2. Specification

2.1 Physical Specifications

2.1.1 Overlook
The overlook views of DiskOnModule are illustrated in Figure 1.

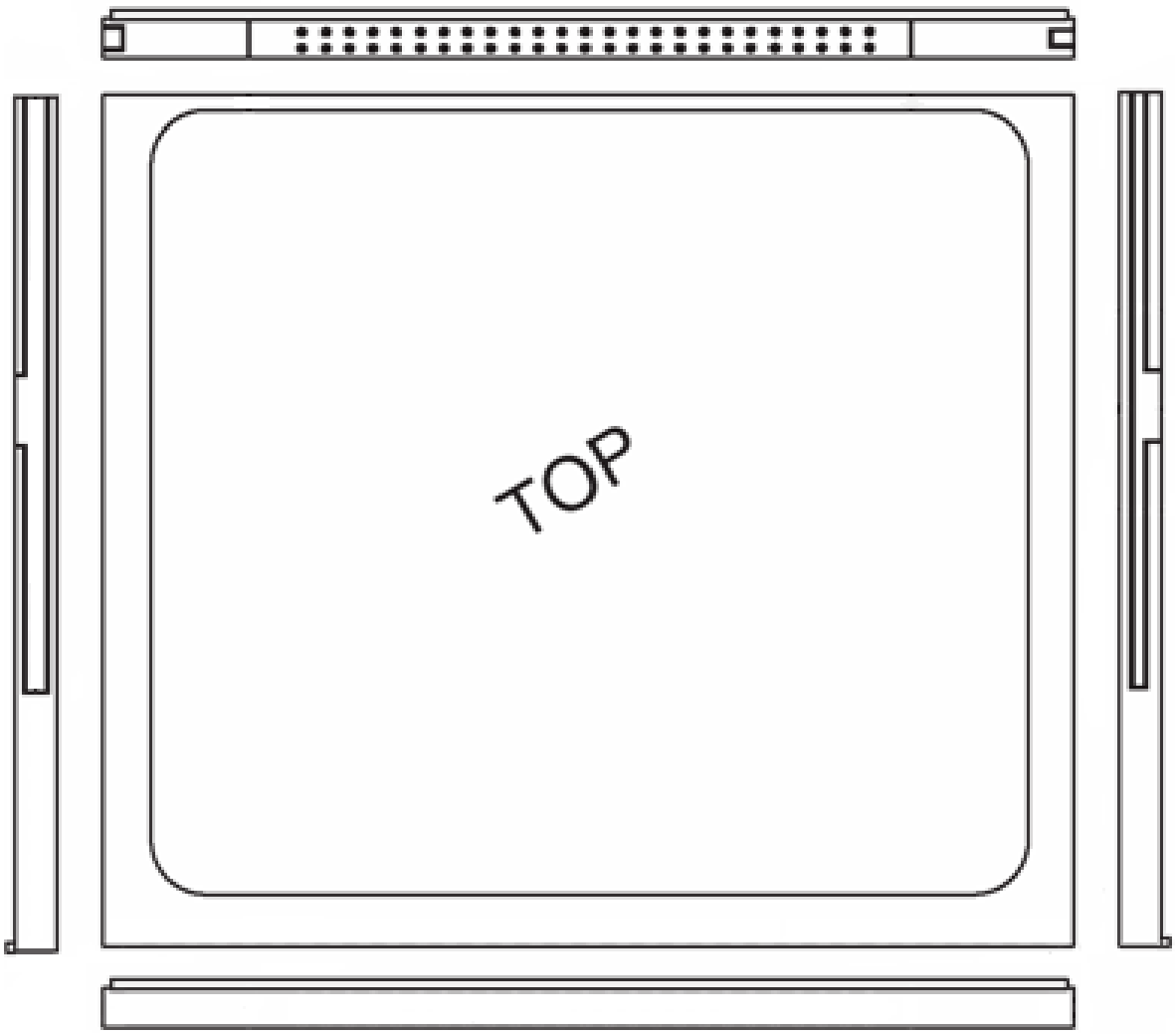


Figure 1: CompactFlash™ Storage Card Overlook Diagram

2.1.2 Dimension

The Dimensions of Compact Flash™ Storage Card are illustrated in Figure 2 and described in Table 1.

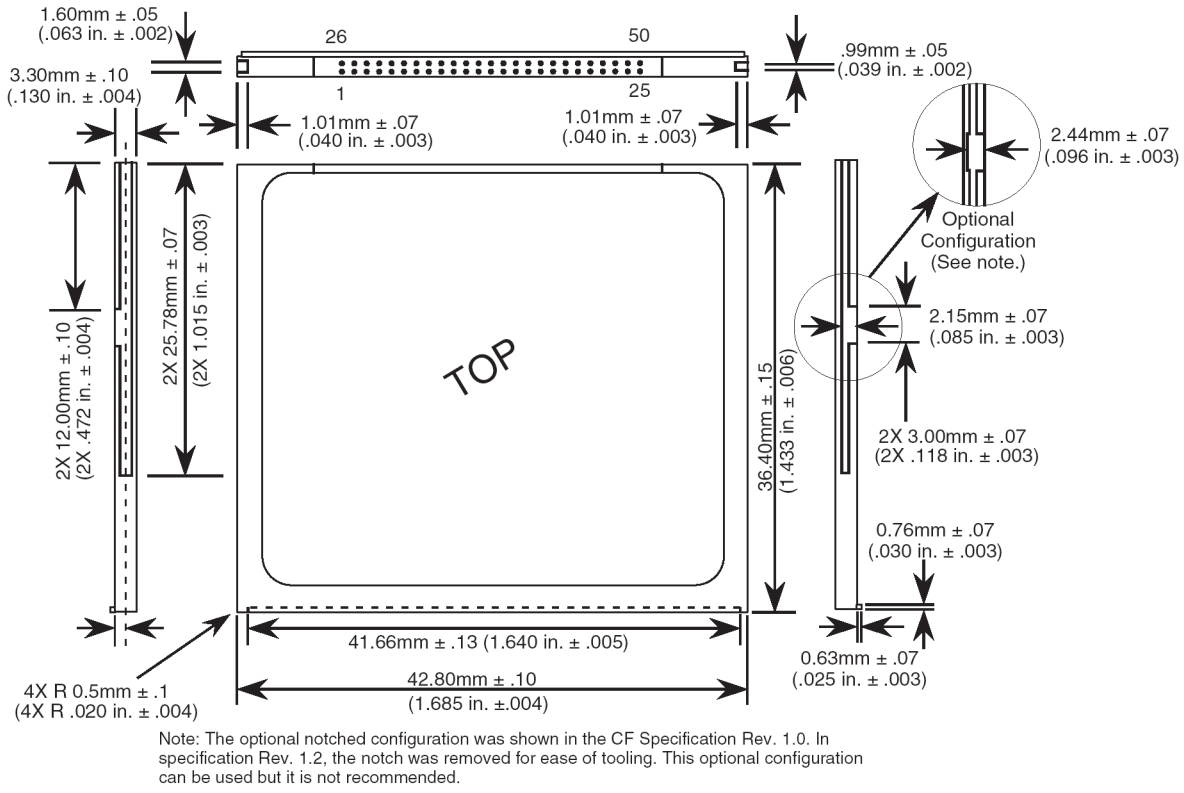


Figure 2: Compact Flash™ Storage Card Dimensions

Notice The optional notched configuration was shown in the CFA specification Rev. 1.0 in specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but is not recommended.

Table 1: Compact Flash™ Storage Card Physical Dimension

Length	36.4 ±0.15 mm (1.433 ±0.006in.)
Width	42.8 ±0.10 mm (1.685 ±0.004in.)
Thickness (Including Label Area)	3.3 ±0.10mm (0.13 ±0.004in)

2.1.3 Weight

- Weight: 11.5g

2.2 Electronic Specifications

2.2.1 Product Definition

The Compact Flash™ Storage Card contains a single chip controller and flash memory module(s) in a matchbook-size package with a 50-pin connector consisting of two rows of 25 female contacts each on 50 mil (1.27mm) centers. The controller interfaces with a host system allowing data to be written to and read from the flash memory modules(s).

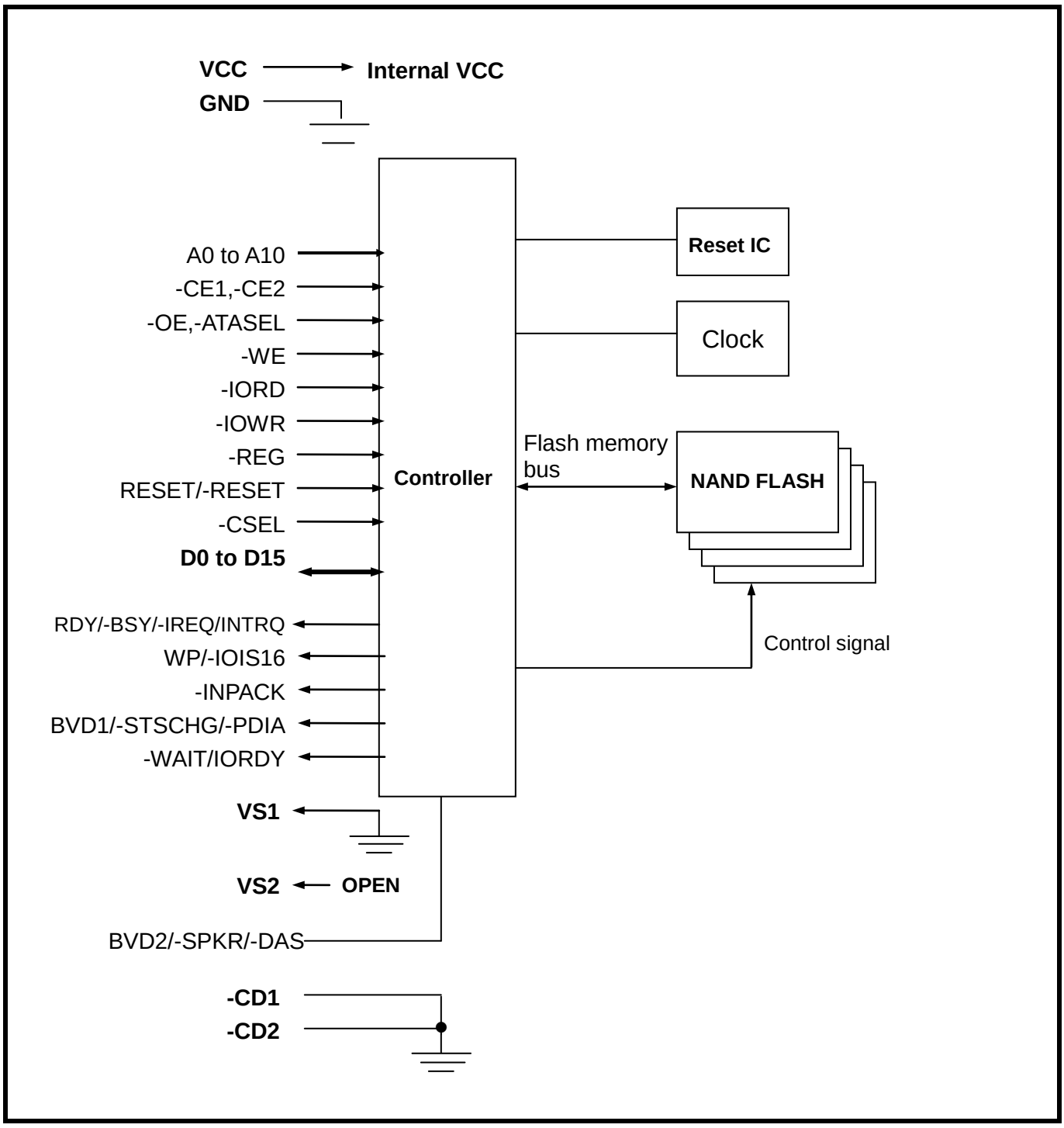


Figure 3: Compact Flash™ Storage Card Block Diagram

2.2.2 Operating Voltage

- Voltage DC +3.3V ± 5% or DC +5.0V ± 10%

2.2.3 Capacity
- Capacity: 128MB~16GB

2.2.4 Power Consumption (3.3V/5.0V)
- Current Information
- Active Mode: 24.1mA / 26.5mA (3.3v / 5.0v)
- Sleep Mode: 200 uA / 300 uA (3.3v/ 5.0v)

2.3 Performance Specifications

2.3.1 Modes
- Memory Card Mode
- I/O Card Mode
- True-IDE Mode
- PIO Mode 4 and Mulit-wordDMA mode2

2.3.2 Data Transfer Time
- Sequential Read: Up to 33MB/s.
- Sequential Write: Up to 20MB/s.

2.3.3 Data Retention
- 10years without requiring power support

Notice The Value of Data Retention is various bases on the type and manufacturer of Flash Memory

2.3.4 Wear-leveling
- Static Wear-Leveling for same level of Write/Erase Cycle

2.3.5 Bad Block Management
- The Bad Blocks of Flash Memory will be replaced into new ones by controller.

2.4 Environmental Specifications

2.4.1 Temperature
- Shock:
  - i. Operating: 1,500G, duration 0.5ms, half sine wave
  - ii. Vibration: 15G peak, 10~2000Hz with 3axis
- Humidity: 0°C~55°C / 95% RH, 10cycles
- Temperature:
  - i. Operating Temperature: -25℃ to +65℃ (Normal)
  - ii. Operating Temperature: -40°C ~ +85°C (Wide Temp)
  - iii. Storage Temperature: -55°C ~ +140°C
- MTBF:1,200,000 Hours
- Fully Compliant with RoHS & REACH directive

2.4.2 Humidity
- Operating Humidity: 8% to 95%
- Non-Operating Humidity: 8% to 95% (with no condensation relative humidity)

2.4.3 Bare Drop Testing
- Testing Conditions: 75cm height
- Testing Orientation: (Free fell) Front/Rear/Right/Left/Top/Bottom side
- Testing Result: Pass

2.4.4 Vibration

- Random Vibration (Operation) : Testing Specification
-

Frequency (Hz)	PSD (G2/Hz)	Acceleration (Grms)	Dwell Time (Min)
10	0.01	6Grms	30min per axis (X・Y・Z)
100	0.08		
500	0.08		

- Random Vibration (Non-Operating): Testing Specification

Frequency (Hz)	PSD (G2/Hz)	Acceleration (Grms)	Dwell Time (Min)
10	0.1	6Grms	30min per axis (X・Y・Z)
100	0.04		
500	0.04		
2000	0.004		

- Frequency Range: 3 ~ 2000Hz
- Testing Result: Pass

2.4.5 Shock and Altitude

T. B. D.

2.5 Reliability Specification

- ECC/EDC (Error Correction Code/Error Detection Code)
- MTBF (Mean Time Between Failure)

2.6 Compliance Specifications

- CE
- FCC

※ Note: Please contact your closest PQI's office for other certificate information.

3. Function

3.1 Pin Signal Assignment

- The signals assigned for Compact Flash Card applications are described in Figure 5 and Table 2;

Figure 4: Compact Flash Storage Card Signal Connector

Table 2 : Compact Flash Storage Card Pin Assignment

Pin No.	Memory card mode		I/O card mode		True IDE mode			
					PIO mode		Multi-word DMA mode	
	Signal name	I/O	Signal name	I/O	Signal name	I/O	Signal name	I/O
1	GND	─	GND	─	GND	─	GND	─
2	D3	I/O	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O	D7	I/O
7	-CE1	I	-CE1	I	-CS0	I	-CS0	I
8	A10	I	A10	I	A10	I	A10	I
9	-OE	I	-OE	I	-ATASEL	I	-ATASEL	I
10	A9	I	A9	I	A9	I	A9	I
11	A8	I	A8	I	A8	I	A8	I
12	A7	I	A7	I	A7	I	A7	I
13	VCC	─	VCC	─	VCC	─	VCC	─
14	A6	I	A6	I	A6	I	A6	I
15	A5	I	A5	I	A5	I	A5	I
16	A4	I	A4	I	A4	I	A4	I
17	A3	I	A3	I	A3	I	A3	I
18	A2	I	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O	D2	I/O
24	WP	O	-IOIS16	O	-IOIS16	O	-IOIS16	O
25	-CD2	O	-CD2	O	-CD2	O	-CD2	O
26	-CD1	O	-CD1	O	-CD1	O	-CD1	O
27	D11	I/O	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O	D15	I/O
32	-CE2	I	-CE2	I	-CS1	I	-CS1	I
33	-VS1	O	-VS1	O	-VS1	O	-VS1	O
34	-IORD	I	-IORD	I	-IORD	I	-IORD	I
35	-IOWR	I	-IOWR	I	-IOWR	I	-IOWR	I
36	-WE	I	-WE	I	-WE	I	-WE	I
37	RDY/-BSY	O	-IREQ	O	INTRQ	O	INTRQ	O
38	VCC	─	VCC	─	VCC	─	VCC	─
39	-CSEL	I	-CSEL	I	-CSEL	I	-CSEL	I
40	-VS2	O	-VS2	O	-VS2	O	-VS2	O
41	RESET	I	RESET	I	-RESET	I	-RESET	I
42	-WAIT	O	-WAIT	O	IORDY	O	IORDY	O
43	-INPACK	O	-INPACK	O	RFU	O	DMARQ	O
44	-REG	I	-REG	I	RFU	I	-DMACK	I
45	BVD2	I/O	-SPKR	I/O	-DASP	I/O	-DASP	I/O
46	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O	-PDIAG	I/O
47	D8	I/O	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O	D10	I/O
50	GND	─	GND	─	GND	─	GND	─

3.2 Card pin Description

Signal Name	Dir	Pin No.	Description
A10 to A0 (PC Card Memory Mode)	I	8,10,11,12,14,15,16,17,18,19,20	These address lines along with the-REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF + Card, the memory mapped port add address registers within the CompactFlash Storage Card or CF+ Card , a byte in the card's information structure and its configuration control and status registers.
A10 to A0 (PC Card I/O Mode)			
A2 to A0 (True IDE Mode)		18,19,20	In True IDE Mode only A {2:0} are used to select the one of eight registers in the Task File. The remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as BVD1 is not supported
-STSCHG (PC Card Memory Mode)			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states; while the I/O interface is configured. Its use is controlled by the Card Configured and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card / I/O Mode)			This line is the Binary AUDIO OUTPUT FROM THE CARD .if the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave
-CD1,-CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompcatFlash Storage Card or CF + Card. They are used by the host to determine that the CompactFlash Storage Card or CF +Card is fully inserted into its socket.
-CE1,-CE2 (PC Card I/O Mode)	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A1.-CE1,-CE2 allows 8 bit hosts to access all data on D0 to D7. See Access specification below.
-CE1,-CE2 (PC Card I/O Mode)			
-CS0,-CS1 (True IDE Mode)			In the True IDE Mode CS0 is the chip select for the task file registers while CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (PC Card Memory Mode	I	39	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pins is open, this device is configured as a Slave.
-CSEL (True IDE Mode)			

Signal Name	Dir	Pin No.	Description
D15 to D00 (PC Card Memory Mode)	I/O	31,30,29,28,27,49,48,47,6,5,4,3,2,23,22,21	These lines carry the Data, Commands and Status information between the host and the controller.D00 is the LSB of the Even Byte of the Word.D08 is the LSB of the Even Byte of the Word.D08 is the LSB of the Odd Byte of the Word.
D15 to D00 (PC Card I/O Mode)			
D15 to D00 (True IDE Mode)			True IDE Mode, all Task File operations occur in byte mode on the low order bus D00 to D07 while all data transfers are 16 bit using D00 to D15.
GND (PC Card Memory Mode)	–	1,50	Ground
GND (PC Card I/O Mode)			
GND (True IDE Mode)			
-INPCAK (PC Card Memory Mode)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode)			The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF +Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF +Card and the CPU.
Reserved (True IDE Mode for PIO)			In True IDE Mode this output signal is not used and should not be connected at the host.
DMARQ (True IDE Mode for Multi-word DMA)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with –DMACK, i.e., the device shall wait until the host asserts –DMACK before negating DMARQ, and reasserting DMARQ if there is more data to transfer. DMARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall not be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA mode and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.

Signal Name	Dir	Pin No.	Description
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF +Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has same function as in PC Card I/O Mode.
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompcatFlash Storage Card or CF +Card controller registers when the CompactFlash Storage Card or CF +Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (Trailing edge)
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF +Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode. This signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
RDY/BSY (PC Card Memory Mode)	O	37	In Memory Mode this signal is set high when the CompactFlash Storage Card or CF +Card is ready to accept a new data transfer operation and held low when the card is busy . The Host memory card socket must provide a pull-up resistor. At power up and at Reset the RDY/-BSY signal is held low (busy) until the CompactFlash Storage Card or CF +Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF +Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true. The CompactFlash Storage Card or CF +Card has been powered up with + RESET continuously disconnected or asserted.
-IREQ (PC Card I/O Mode)			Operation-After the CompactFlash Storage Card or CF + Card has been configured for I/O operation; this signal is used as interrupt Request. This line is strobe low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high interrupt Request to the host.

Signal Name	Dir	Pin No.	Description
-REG (PC Card Memory Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register(Attribute) Memory accesses. High for Common Memory. Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
Reserved (True IDE Mode for PIO)			In the True IDE Mode, this input signal is not used and should be driven high or connected to VCC by the host.
-DMACK (True IDE Mode for Multi-word DMA)			This is a DMA acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the –DMACK signal, including a floating condition. If DMA operation is not supported by a True-IDE mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
RESET (PC Card Memory Mode)	I	41	When the pin is high, this signal Resets the CompactFlash Storage Card or CF +Card. The CompcatFlash Storage Card or CF +Card is Reset only at power up if this pin is left high or open from power-up. The CompactFlash Storage Card or CF +Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset form the host.
VCC (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	–	13,38	+5V +3.3V power.
-VS1 /-VS2 (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	O	33,40	Voltage Sense Signals. –VS1 is grounded so that the CompactFlash Storage Card or CF + Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage.
-WAIT (PC Card Memory Mode)	O	42	The –WAIT signal is driven low by the CompactFlash Storage Card or CF +Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O Mode)			
IORDY (True IDE Mode)			In True IDE Mode this output signal may be used as IORDY.

Signal Name	Dir	Pin No.	Description
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for starting memory write data to the registers of the CompactFlash Storage Card or CF + Card when the card is configured I the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	O	24	Memory Mode-The CompactFlash Storage Card or CF + Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation-When the CompactFlash Storage Card or CF + Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOIS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

3.3 Access specification

3.3.1 Attribute access specifications

When CIS-ROM region or Configuration register region is accessed, read and write operations are executed under the condition of –REG = “L” as follows. That region can be accessed by Byte/Word/Odd-byte modes, which are defined by PC card standard specifications.

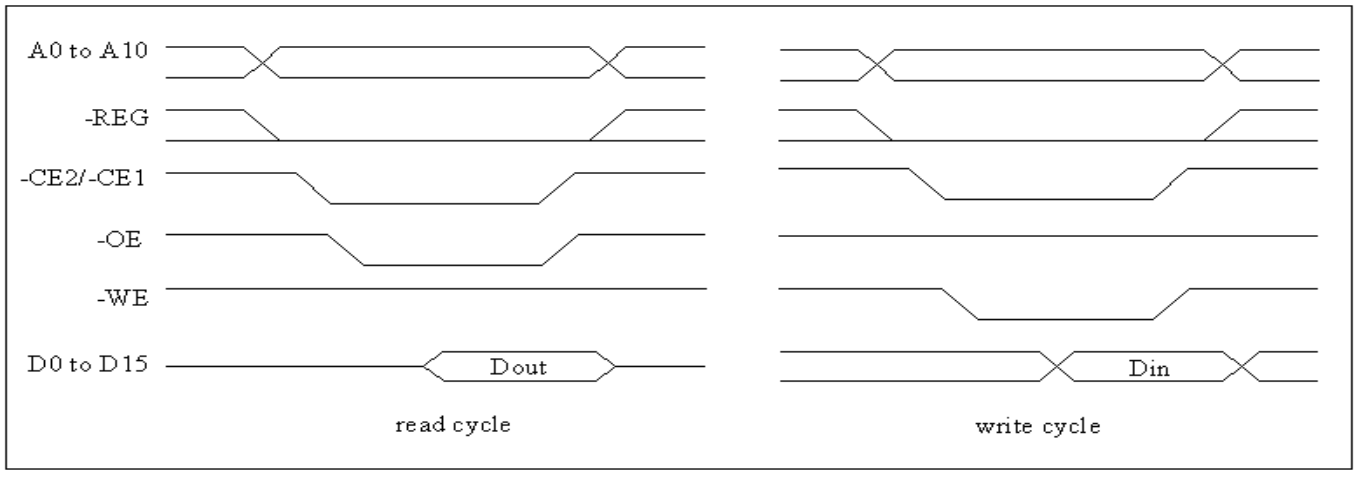
Attribute Read Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	High-Z	High-Z
Byte access (8-it)	L	H	L	L	L	H	High-Z	even byte
	L	H	L	H	L	H	High-Z	invalid
Word access (16-it)	L	L	L	X	L	H	invalid	even byte
Odd byte access (8bit)	L	L	H	X	L	H	invalid	High-Z
Note: X → L or H								

Attribute Write Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	Don’t care	Don’t care
Byte access (8bit)	L	H	L	L	H	L	Don’t care	even byte
	L	H	L	H	H	L	Don’t care	Don’t care
Word access (16bit)	L	L	L	×	H	L	Don’t care	even byte
Odd byte access (8bit)	L	L	H	×	H	L	Don’t care	Don’t care
Note: X → L or H								

Attribute Access Timing Example



3.3.2 Task file Register access specifications

There are two cases of Task File register mapping, one is mapped I/O address area, the other is mapped Memory address area. Each case of Task File registers read and write operations is executed under the condition as follows. That area can be accessed by Byte/World/Odd Byte modes, which are defined by PC card standard specifications.

3.3.2.1 I/O address map

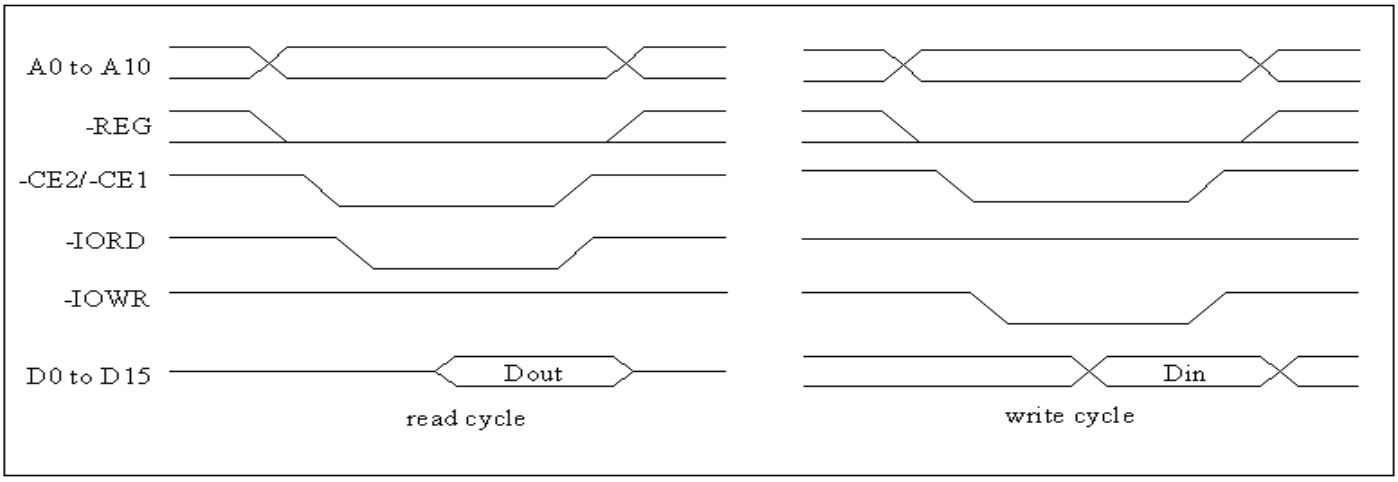
Task File Register Read Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	High-Z	High-Z
Byte access (8bit)	L	H	L	L	L	H	H	H	High-Z	even byte
	L	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16bit)	L	L	L	X	L	H	H	H	odd byte	even byte
Odd byte access (8bit)	L	L	H	X	L	H	H	H	odd byte	High-Z
Note: X→ L or H										

Task File Register Write Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	Don't care	Don't care
Byte access(8-bit)	L	H	L	L	H	L	H	H	Don't care	even byte
	L	H	L	H	H	L	H	H	Don't care	odd byte
Word access(16-bit)	L	L	L	×	H	L	H	H	odd byte	even byte
Odd byte access(8-bit)	L	L	H	×	H	L	H	H	odd byte	don't care
Note: X→ L or H										

Task File Register Access Timing Example (1)



3.3.2.2 Memory address map

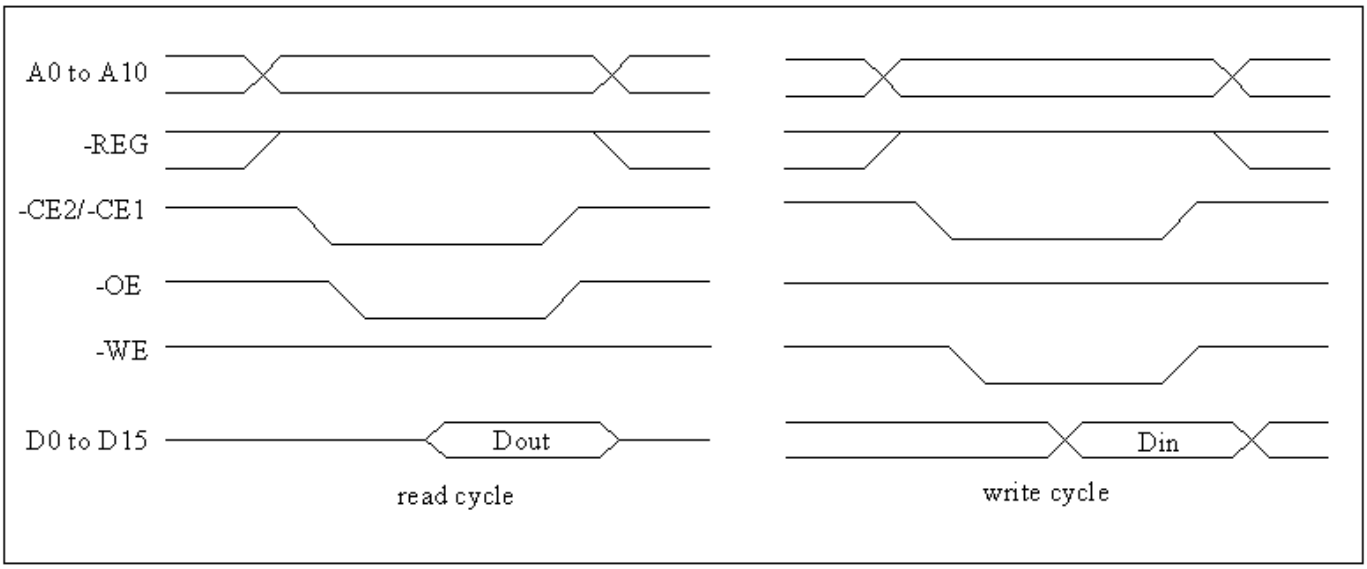
Task File Register Read Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	High-Z	High-Z
Byte access (8bit)	H	H	L	L	L	H	H	H	High-Z	even byte
	H	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16bit)	H	L	L	X	L	H	H	H	odd byte	even byte
Odd byte access (8bit)	H	L	H	X	L	H	H	H	odd byte	High-Z
Note: X→ L or H										

Task File Register Write Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	X	H	H	X	X	X	X	X	Don't care	Don't care
Byte access (8bit)	H	H	L	L	H	L	H	H	Don't care	even byte
	H	H	L	H	H	L	H	H	Don't care	odd byte
Word access (16bit)	H	L	L	X	H	L	H	H	odd byte	even byte
Odd byte access (8bit)	H	L	H	X	H	L	H	H	odd byte	don't care
Note: X→ L or H										

Task File Register Access Timing Example (2)



3.3.2.3 True IDE Mode

The card can be configured in a True IDE This card is configured in this mode only when the –OE input signal is asserted GND by the host. In this True IDE mode Attribute Registers are not accessible from the host. Only I/O operation to the task file and data register is allowed. If this card is configured during power on sequence, data register is accessed in word (16-bit). The card permits 8-bit accessed if the user issues a Set Feature Command to put the device in 8-bit mode.

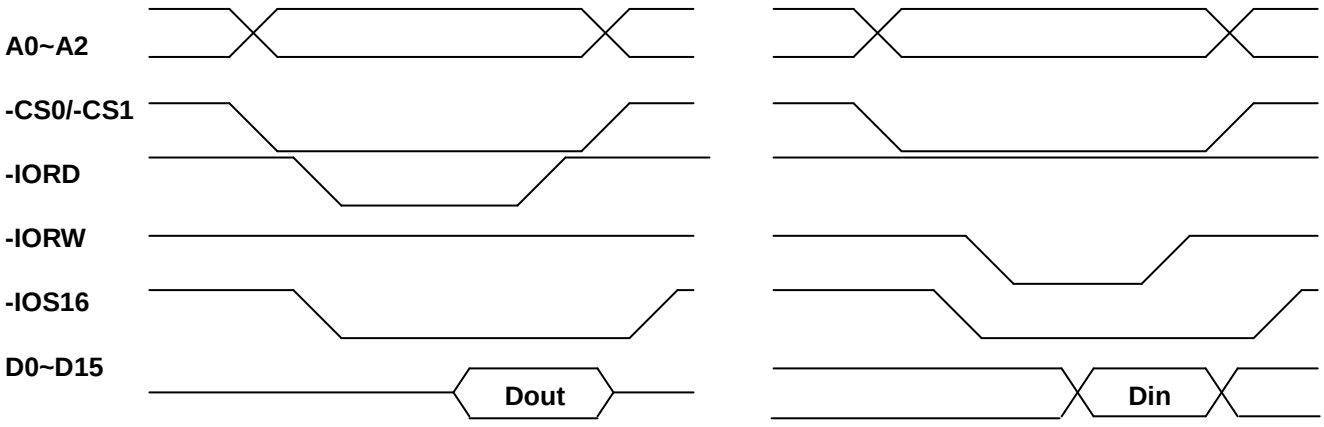
True IDE Mode Read I/O Function

Mode	-CS1	-CS0	A0~A2	-IORD	-IOWR	D8 to D15	D0 to D7
Invalid mode	L	L	X	X	X	High-Z	High-Z
Standby mode	H	H	X	X	X	High-Z	High-Z
Data register access	H	L	0	L	H	Odd byte	even byte
Alternate status access	L	H	6H	L	H	High-Z	Status out
Other task file access	H	L	1~7H	L	H	High-Z	Data
Note: X→ L or H							

True IDE Mode Write I/O Function

Mode	-CS1	-CS0	A0~A2	-IORD	-IOWR	D8 to D15	D0 to D7
Invalid mode	L	L	X	X	X	Don't card	Don't card
Standby mode	H	H	X	X	X	Don't card	even byte
Data register access	H	L	0	H	L	Odd byte	Don't card
Alternate status access	L	H	6H	H	L	Don't card	Control in
Other task file access	H	L	1~7H	H	L	Odd byte	Data
Note: X→ L or H							

True IDE Mode I/O Access Timing Example



3.3.3 Configuration register specification

This Compact Flash card supports four Configuration registers for the purpose of the configuration and observation of this card.

3.3.3.1 Configuration Option register (Address 200H)

This register is used for the configuration of the card configuration status and for the issuing soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRESET	LevIREQ	INDEX					
Note: initial value: 00H							

Name	R/W	Function
SRESET (HOST->)	R/W	Setting this bit to “1”, places the card in the reset state (Card Hard Reset). This operation is equal to Hard Reset, except this bit is not cleared. Then this bit set to “0”,places the card in the reset state of Hard Reset (This bit is set to “0” by Hard Reset). Card configuration status is reset and the card internal initialized operation starts when Card Hard Reset is executed, so next access to the card should be the same sequence as the power on sequence.
LevIREQ (HOST->)	R/W	This bit sets to “0” when pulse mode interrupt is selected and “1 when level mode interrupt is selected.
INDEX (HOST->)	R/W	This bits is used for select operation mode of the card as follows. When Power on, Card Hard Reset and Soft Reset, this data is “000000” for the purpose of Memory card interface recognition.
Note: initial value → 00H		

INDEX bit assignment

INDEX bit								
5	4	3	2	1	0	Card mode	Task File register address	Mapping mode
0	0	0	0	0	0	Memory card	0H to FH, 400H to 7FFH	memory mapped
0	0	0	0	0	1	I/O card	××0H to ××FH	Contiguous I/O mapped
0	0	0	0	1	0	I/O card	1F0H to 1F7H, 3F6H to 3F7H	Primary I/O mapped
0	0	0	0	1	1	I/O card	170H to 177H, 376H to 377H	Secondary I/O mapped

3.3.3.2 Configuration and Status register (Address 202H)

This register is used for observing the card state.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0
Note: initial value: 00H							

Name	R/W	Function
CHGED (CARD->)	R	This bit indicates that CRDY-BSY bit on Pin Replacement register is set to “1”. When CHGED bit is set to “1”, -STSCHG pin is held “L” at the confition of SIGCHG bit set to “1” and the card configured for the I/O interface.
SIGCHG (HOST->)	R/W	This bit is set or reset by the host for enabling and disabling the status-change signal (-STSCHG pin). When the card is configured I/O card interface and this bit is set to “1”, -STSCHG pin is controlled by CHGED bit. If this bit is set to “0”, -STSCHG pin is kept “H”.

IOIS8 (HOST->)	R/W	The host sets this field to “1” when it can provide I/O cycles only with on 8bit data bus (D7 to D0).
PWD (HOST->)	R/W	When this bit is set to “1”, the card enters sleep state (Power Down mode). When this bit is reset to “0”, the card transfers to idle state (active mode). RRDY/-BSY bit on Pin Replacement Register becomes BUSY when this bit is changed. RRDY/-BSY will not become Ready until the power state requested has been entered. This card automatically powers down when it is idle, and powers back up when it receives a command.
INTR (CARD->)	R	This bit indicates the internal state of the interrupt request. This bit state is available whether I/O card interface has been configured or not. This signal remains true until the condition which cased the interrupt request has been serviced. If interrupts are disabled by the –IEN bit in the Device Control Register, this bit is a zero.

3.3.3.3 Pin Replacement register (Address 204H)

This register is used for providing the signal state of –IREQ signal when the card configured I/O card interface.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	CRDY/-BSY	0	1	1	RRDY/-BSY	0
Note: initial value: 00H							

Name	R/W	Function
CRDY/-BSY (HOST->)	R/W	This bit is set to “1” when the RRDY/-BSY bit changes state. This bit may also be written by the host.
RRDY/-BSY (HOST->)	R/W	When read, this bit indicates +READY pin states. When written, this bit is used for CRDY/-Bsy bit masking.

3.3.3.4 Socket and Copy register (Address 206H)

This register is used for identification of the card from the other card. Host can read and write this register. This register should be set by host before this card’s Configuration Option register set.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	DRV#	0	0	0	0
Note: initial value: 00H							

Name	R/W	Function
DRV# (HOST->)	R/W	These fields are used for the configuration of the plural cards. When host configures the plural cards, written the card’s copy number in this field. In this way, host can perform the card’s master/slave organization.

3.3.4 CIS Information

CIS information of Compact Flash Card are defined as follows.

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
000H	01H	CISTPL_DEVICE								Device Info tuple	Tuple code
002H	03H	TPL_LINK								Link length is 3 byte	Link to next tuple
004H	D9H	Device Type				W	Speed			Type=D: I/O device WPS=1: no WP switch Speed=1: 250 ns	Device type, WPS, speed
006H	01H	# address units –1					unit size			2 Kbytes of address space	Device size
008H	FFH	CISTPL_END								End of CISTPL_DEVICE	End marker
00AH	1Ch	CISTPL_DEVICE_OC								Common memory other operating conditions tuple	Tuple code
00CH	04H	TPL_LINK								Link length is 4 byte	Link to next tuple
00EH	02H	Ext	Reserved					3V	M	3V=1: dual voltage card, conditions for 3.3V operation M=0: conditions without wait	Other Conditions Information
010H	D9H	Device Type				W	Speed			Type=D: I/O device WPS=1: no WP switch Speed=1: 250 ns	Device type, WPS, speed
012H	01H	# address units –1					unit size			2 Kbytes of address space	Device size
014H	FFH	CISTPL_END								End of CISTPL_DEVICE_OC	End marker
016H	18H	CISTPL_JEDEC_C								JEDEC programming info tuple	Tuple code
018H	02H	TPL_LINK								Link length is 2 byte	Link to next tuple
01AH	DFH	JEDEC ID								Device manufacturer ID	Manufacturer ID
01CH	01H	JEDEC Info								Manufacturer specific info	Manufacturer info
01EH	20H	CISTPL_MANFID								Manufacturer ID tuple	Tuple code
020H	04H	TPL_LINK								Link length is 4 bytes	Link to next tuple
022H	00H	TPLMID_MANF								PC Card manufacturer code	Manufacturer ID
024H	00H										
026H	00H	TPLMID_CARD								Manufacturer specific info	Manufacturer info
028H	00H										
02AH	21H	CISTPL_FUNCID								Function ID tuple	Tuple code
02CH	02H	CISTPL_LINK								Link length is 2 bytes	Link to next tuple
02EH	04H	TPLFID_FUNCTION								Fixed disk drive	Function code
030H	01H	Reserved						R	P	R=0: no expansion ROM P=1: configure at POST	System init byte TPLFID_SYSINIT
032H	22H	CISTPL_FUNCE								Function Extension tuple	Tuple code
034H	02H	CISTPL_LINK								Link length is 2 bytes	Link to next tuple
036H	01H	Disk function extension tuple								Disk interface information	TPLFE_TYPE
038H	01H	Disk interface type								PC card ATA interface	TPLFE_DATA
03AH	22H	CISTPL_FUNCE								Function Extension tuple	Tuple code
03CH	03H	CISTPL_LINK								Link length is 3 bytes	Link to next tuple

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
03EH	02H	Disk function extension tuple								PC card ATA basic features	TPLFE_TYPE
040H	04H	Reserved			D	U	S	V		D=0: single drive on card U=0: no unique serial number S=1: silicon device V=0: no V_{PP} required	TPLFE_TYPE
042H	07H	R	I	E	N	P				I=0: twin IOIS16# unspecified E=0: index bit not emulated N=0: I/O includes 0x3F7 P=7: sleep, standby, idle supported	TPLFE_TYPE
044H	1AH	CISTPL_CONFIG								Configuration Tuple	Tuple code
046H	05H	TPL_LINK								Link length is 5 bytes	Link to next tuple
048H	01H	RFS		RMS				RAS		RFS: reserved RMS: 1 byte register mask RAS: 2 bytes base address	Size of fields TPCC_SZ
04AH	07H	TPCC_LAST								Last configuration entry is 07H	Last entry index
04CH	00H	TPCC_RADR (LSB)								Configuration registers are located at 0200H	Configuration register location
04EH	02H	TPCC_RADR (MSB)									
050H	0FH	TPCC_RMSK								Configuration registers 0 to 3 are present	Configuration reg-ister present mask
052H	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
054H	0BH	CISTPL_LINK								Link length is 11 bytes	Link to next tuple
056H	C0H	I	D	Configuration Index						Memory mapped configuration, index=0 I=1: Interface byte follows D=1: Default entry	Configuration Table Index Byte TPCE_INDX
058H	C0H	W	R	P	B	Interface type				W=1: wait required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=0: Memory interface	Interface Description TPCE_IF
05AH	A1H	M	MS		IR	IO	T	Power		M=1: misc info present MS=1: 2 byte memory length IR=0: no interrupt is used IO=0: no I/O space is used T=0: no timing info specified Power=1: V_{CC} info, no V_{PP}	Feature Selection Byte TPCE_FS
05CH	27H	R	DI	PI	AI	SI	HV	LV	NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	Power Description Structure Parameter Selection Byte TPCE_PD
05EH	55H	X	Mantissa				Exponent			Nominal voltage 5.0V	
060H	4DH	X	Mantissa				Exponent			Minimum voltage 4.5V	
062H	5DH	X	Mantissa				Exponent			Maximum voltage 5.5V	
064H	75H	X	Mantissa				Exponent			Peak current 80 mA	

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
066H	08H	Length in 256 byte units (LSB)								Length of memory space is 2 Kbytes	Memory space- descr. TPCE_MS
068H	00H	Length in 256 byte units (MSB)									
06AH	21H	X	R	P	RO	A	T			X=0: no more misc fields P=1: power-down supported RO=0:read/write media A=0: audio not supported T=1: max twins is 1	Miscellaneous features TPCE_MI
06CH	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
06EH	06H	CISTPL_LINK								Link length is 6 bytes	Link to next tuple
070H	00H	I	D	Configuration Index						Memory mapped configuration, index=0	TPCE_INDX
072H	01H	M	MS		IR	IO	T	Power		Power=1: V_{CC} info, no V_{PP}	TPCE_FS
074H	21H	R	DI	PI	AI	SI	HV	LV	NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
076H	B5H	X	Mantissa				Exponent			X=1: extension byte present	
078H	1EH	X	Extension							Nominal voltage 3.30V	
07AH	4DH	X	Mantissa				Exponent			Peak current 45 mA	
07CH	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
07EH	0DH	CISTPL_LINK								Link length is 13 bytes	Link to next tuple
080H	C1H	I	D	Configuration Index						I/O mapped, index=1 I=1: Interface byte follows D=1: Default entry	TPCE_INDX
082H	41H	W	R	P	B	Interface type				W=0: wait not required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=1: I/O interface	TPCE_IF
084H	99H	M	MS		IR	IO	T	Power		M=1: misc info present MS=0: no memory space info IR=1: interrupt is used IO=1: I/O space is used T=0: no timing info specified Power=1: V_{CC} info, no V_{PP}	TPCE_FS
086H	27H	R	DI	PI	AI	SI	HV	LV	NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	TPCE_PD
088H	55H	X	Mantissa				Exponent			Nominal voltage 5.0V	
08AH	4DH	X	Mantissa				Exponent			Minimum voltage 4.5V	
08CH	5DH	X	Mantissa				Exponent			Maximum voltage 5.5V	
08EH	75H	X	Mantissa				Exponent			Peak current 80 mA	
090H	64H	R	S	E	IO					S=1: support 16 bit hosts E=1: support 8 bit hosts IO=4: 4 address lines decoded	TPCE_IO

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
092H	F0H	S	P	L	M	V	B	I	N	S=1: interrupt sharing logic P=1: pulse mode supported L=1: level mode supported M=1: masks V..N present V=0: no vendor unique IRQ B=0: no bus error IRQ I=0: no I/O check IRQ N=0: no NMI	TPCE_IR
094H	FFH	IRQ7..0								Interrupt signal may be assigned to any host IRQ	
096H	FFH	IRQ15..8									
98H	21H	X	R	P	RO	A	T			X=0: no more misc fields P=1: power-down supported RO=0:read/write media A=0: audio not supported T=1: max twins is 1	TPCE_MI
09AH	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
09CH	06H	CISTPL_LINK								Link length is 6 bytes	Link to next tuple
09EH	01H	I	D	Configuration Index						I/O mapped, index=1	TPCE_INDX
0A0H	01H	M	MS		IR	IO	T	Power		Power=1: V_{CC} info, no V_{PP}	TPCE_FS
0A2H	21H	R	DI	PI	AI	SI	HV	LV	NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
0A4H	B5H	X	Mantissa				Exponent			X=1: extension byte present	
0A6H	1EH	X	Extension							Nominal voltage 3.30V	
0A8H	4DH	X	Mantissa				Exponent			Peak current 45 mA	
0AAH	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
0ACH	12H	CISTPL_LINK								Link length is 18 bytes	Link to next tuple
0AEH	C2H	I	D	Configuration Index						I/O mapped, index=2 I=1: Interface byte follows D=1: Default entry	TPCE_INDX
0B0H	41H	W	R	P	B	Interface type				W=0: wait not required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=1: I/O interface	TPCE_IF
0B2H	99H	M	MS		IR	IO	T	Power		M=1: misc info present MS=0: no memory space info IR=1: interrupt is used IO=1: I/O space is used T=0: no timing info specified Power=1: V_{CC} info, no V_{PP}	TPCE_FS
0B4H	27H	R	DI	PI	AI	SI	HV	LV	NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	TPCE_PD
0B6H	55H	X	Mantissa				Exponent			Nominal voltage 5.0V	
0B8H	4DH	X	Mantissa				Exponent			Minimum voltage 4.5V	
0BAH	5DH	X	Mantissa				Exponent			Maximum voltage 5.5V	

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
0BCH	75H	X	Mantissa				Exponent			Peak current 80 mA	
0BEH	EAH	R	S	E	IO					R=1: range follows S=1: support 16 bit hosts E=1: support 8 bit hosts IO=10: 10 lines decoded	TPCE_IO
0C0H	61H	LS		AS		NR				LS=1: 1 byte length AS=2: 2 byte address NR=1: 2 address ranges	
0C2H	F0H	Base address 1 (LSB)								Address range 1 0x1F0 to 0x1F7	
0C4H	01H	Base address 1 (MSB)									
0C6H	07H	Address range 1 length									
0C8H	F6H	Base address 2 (LSB)								Address range 2 0x3F6 to 0x3F7	
0CAH	03H	Base address 2 (MSB)									
0CCH	01H	Address range 2 length									
0CEH	EEH	S	P	L	M	IRQN				S=1: interrupt sharing logic P=1: pulse mode supported L=1: level mode supported M=0: masks V..N not present IRQN=14: use interrupt 14	TPCE_IR
0D0H	21H	X	R	P	RO	A	T			X=0: no more misc fields P=1: power-down supported RO=0:read/write media A=0: audio not supported T=1: max twins is 1	TPCE_MI
0D2H	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
0D4H	06H	CISTPL_LINK								Link length is 6 bytes	Link to next tuple
0D6H	02H	I	D	Configuration Index						I/O mapped, index=2	TPCE_INDX
0D8H	01H	M	MS		IR	IO	T	Power		Power=1: V_{CC} info, no V_{PP}	TPCE_FS
0DAH	21H	R	DI	PI	AI	SI	HV	LV	NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
0DCH	B5H	X	Mantissa				Exponent			X=1: extension byte present	
0DEH	1EH	X	Extension							Nominal voltage 3.30V	
0E0H	4DH	X	Mantissa				Exponent			Peak current 45 mA	
0E2H	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
0E4H	12H	CISTPL_LINK								Link length is 18 bytes	Link to next tuple
0E6H	C3H	I	D	Configuration Index						I/O mapped, index=3 I=1: Interface byte follows D=1: Default entry	TPCE_INDX
0E8H	41H	W	R	P	B	Interface type				W=0: wait not required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=1: I/O interface	TPCE_IF
0EAH	99H	M	MS		IR	IO	T	Power		M=1: misc info present MS=0: no memory space info IR=1: interrupt is used IO=1: I/O space is used T=0: no timing info specified Power=1: V_{CC} info, no V_{PP}	TPCE_FS

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
0ECH	27H	R	DI	PI	AI	SI	HV	LV	NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	TPCE_PD
0EEH	55H	X	Mantissa				Exponent			Nominal voltage 5.0V	
0F0H	4DH	X	Mantissa				Exponent			Minimum voltage 4.5V	
0F2H	5DH	X	Mantissa				Exponent			Maximum voltage 5.5V	
0F4H	75H	X	Mantissa				Exponent			Peak current 80 mA	
0F6H	EAH	R	S	E	IO					R=1: range follows S=1: support 16 bit hosts E=1: support 8 bit hosts IO=10: 10 lines decoded	TPCE_IO
0F8H	61H	LS		AS	NR					LS=1: 1 byte length AS=2: 2 byte address NR=1: 2 address ranges	
0FAH	70H	Base address 1 (LSB)								Address range 1 0x170 to 0x177	
0FCH	01H	Base address 1 (MSB)									
0FEH	07H	Address range 1 length									
100H	76H	Base address 2 (LSB)								Address range 2 0x376 to 0x377	
102H	03H	Base address 2 (MSB)									
104H	01H	Address range 2 length									
106H	EEH	S	P	L	M	IRQN				S=1: interrupt sharing logic P=1: pulse mode supported L=1: level mode supported M=0: masks V..N not present IRQN=14: use interrupt 14	TPCE_IR
108H	21H	X	R	P	RO	A	T			X=0: no more misc fields P=1: power-down supported RO=0:read/write media A=0: audio not supported T=1: max twins is 1	TPCE_MI
10AH	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
10CH	06H	CISTPL_LINK								Link length is 6 bytes	Link to next tuple
10EH	03H	I	D	Configuration Index						I/O mapped, index=3	TPCE_INDX
110H	01H	M	MS		IR	IO	T	Power		Power=1: V_{CC} info, no V_{PP}	TPCE_FS
112H	21H	R	DI	PI	AI	SI	HV	LV	NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
114H	B5H	X	Mantissa				Exponent			X=1: extension byte present	
116H	1EH	X	Extension							Nominal voltage 3.30V	
118H	4DH	X	Mantissa				Exponent			Peak current 45 mA	
11AH	1BH	CISTPL_CFTABLE_ENTRY								Configuration tuple	Tuple code
11CH	04H	CISTPL_LINK								Link length is 4 bytes	Link to next tuple
11EH	07H	I	D	Configuration Index						I/O mapped, index=7	TPCE_INDX
120H	00H	M	MS		IR	IO	T	Power		No feature descriptions follow	TPCE_FS

Address	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS function
122H	28H									Hyperstone specific data	
124H	D3H									Hyperstone specific data	
126H	14H	CISTPL_NO_LINK								No link control tuple	Tuple code
128H	00H	CISTPL_LINK								Link length is 0 bytes	Link to next tuple
12AH	15H	CISTPL_VERS_1								Level 1 version/product info	Tuple code
12CH	0AH	CISTPL_LINK								Link length is 21 bytes	Link to next tuple
12EH	04H	TPPLV1_MAJOR								PCMCIA2.0/JEIDA4.1	Major version
130H	01H	TPPLV1_MINOR								PCMCIA2.0/JEIDA4.1	Minor version
132H	20H										
134H	20H										
136H	20H										
138H	20H										
13AH	20H										
13CH	00H									Null terminator	
13EH	20H										Info string “ “
140H	00H									Null terminator	
142H	FFH										
144H	FFH										
146H	FFH										
148H	FFH										
14AH	FFH										
14CH	FFH										
14EH	FFH										
150H	FFH										
152H	FFH										
154H	FFH										
156H	FFH	CISTPL_END								End of CISTPL_VERS_1	End marker
158H	FFH	CISTPL_END								End of CIS	Tuple code

3.3.5 Task file register specification

There registers are used for reading and writing the storage data in this card. These registers are mapped five types by the configuration of INDEX in Configuration Option register. The decoded addressed are shown as follows.

Memory map (INDEX=0)

-REG	A10	A9~A4	A3	A2	A1	A0	Offset	-OE=L	-WE=L
1	0	X	0	0	0	0	0H	Data register	Data register
1	0	X	0	0	0	1	1H	Error register	Feature register
1	0	X	0	0	1	0	2H	Select count register	Sector count register
1	0	X	0	0	1	1	3H	Sector number register	Sector number register
1	0	X	0	1	0	0	4H	Cylinder lox register	Cylinder low register
1	0	X	0	1	0	1	5H	Cylinder high register	Cylinder high register
1	0	X	0	1	1	0	6H	Drive head register	Drive head register
1	0	X	0	1	1	1	7H	Status register	Command register
1	0	X	1	0	0	0	8H	Dup. Even data register	Dup. Even data register
1	0	X	1	0	0	1	9H	Dup. Odd data register	Dup. Odd data register
1	0	X	1	1	0	1	DH	Dup. Error register	Dup. Feature register
1	0	X	1	1	1	0	EH	Alt. Status register	Dup. Feature register
1	0	X	1	1	1	1	FH	Drive address register	Reserved
1	0	X	X	X	X	0	8H	Even data register	Even data register
1	0	X	X	X	X	1	9H	Odd data register	Odd data register

Contiguous I/O map (INDEX=1)

-REG	A10~A4	A3	A2	A1	A0	Offset	-OE=L	-WE=L
0	X	0	0	0	0	0H	Data register	Data register
0	X	0	0	0	1	1H	Error register	Feature register
0	X	0	0	1	0	2H	Select count register	Sector count register
0	X	0	0	1	1	3H	Sector number register	Sector number register
0	X	0	1	0	0	4H	Cylinder lox register	Cylinder low register
0	X	0	1	0	1	5H	Cylinder high register	Cylinder high register
0	X	0	1	1	0	6H	Drive head register	Drive head register
0	X	0	1	1	1	7H	Status register	Command register
0	X	1	0	0	0	8H	Dup. Even data register	Dup. Even data register
0	X	1	0	0	1	9H	Dup. Odd data register	Dup. Odd data register
0	X	1	1	0	1	DH	Dup. Error register	Dup. Feature register
0	X	1	1	1	0	EH	Alt. Status register	Dup. Feature register
0	X	1	1	1	1	FH	Drive address register	Reserved

Primary map (INDEX=2)

-REG	A10	A9~A4	A3	A2	A1	A0	-IORD=L	-IOWR=L
0	X	1FH	0	0	0	0	Data register	Data register
0	X	1FH	0	0	0	1	Error register	Feature register
0	X	1FH	0	0	1	0	Select count register	Sector count register
0	X	1FH	0	0	1	1	Sector number register	Sector number register
0	X	1FH	0	1	0	0	Cylinder lox register	Cylinder low register
0	X	1FH	0	1	0	1	Cylinder high register	Cylinder high register
0	X	1FH	0	1	1	0	Drive head register	Drive head register
0	X	1FH	0	1	1	1	Status register	Command register
0	X	1FH	0	1	1	0	Alt. Status register	Device control register
0	X	1FH	0	1	1	1	Drive address register	Reserved

Secondary I/O map (INDEX=3)

-REG	A10	A9~A4	A3	A2	A1	A0	-IORD=L	-IOWR=L
0	X	17H	0	0	0	0	Data register	Data register
0	X	17H	0	0	0	1	Error register	Feature register
0	X	17H	0	0	1	0	Select count register	Sector count register
0	X	17H	0	0	1	1	Sector number register	Sector number register
0	X	17H	0	1	0	0	Cylinder lox register	Cylinder low register
0	X	17H	0	1	0	1	Cylinder high register	Cylinder high register
0	X	17H	0	1	1	0	Drive head register	Drive head register
0	X	17H	0	1	1	1	Status register	Command register
0	X	37H	0	1	1	0	Alt. Status register	Device control register
0	X	37H	0	1	1	1	Drive address register	Reserved

True IDE Mode I/O map

-CS1	-CS0	A2	A1	A0	-INRD=L	-IOWR=L
1	0	0	0	0	Data register	Data register
1	0	0	0	1	Error register	Feature register
1	0	0	1	0	Select count register	Sector count register
1	0	0	1	1	Sector number register	Sector number register
1	0	1	0	0	Cylinder lox register	Cylinder low register
1	0	1	0	1	Cylinder high register	Cylinder high register
1	0	1	1	0	Drive head register	Drive head register
1	0	1	1	1	Status register	Command register
0	1	1	1	0	Alt. Status register	Device control register
0	1	1	1	1	Drive address register	Reserved

1. Data register

This register is a 16-bit register that has read/write ability. And it is used for transferring 1 sector data between the card and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error or Feature register**.**

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D0 to D15															

2. Error register

This register is a read only register, and it is used for analyzing the error content at the card accessing. This register is valid when the BSY bit in Status register and Alternate Status register are set to “0”(Ready).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

bit	Name	Function
7	BBK(Bad Block detected)	This bit set when a Bad is detected in requester ID field.
6	UNC(Data ECC error)	This bit is set when Uncorrectable error is occurred at reading the card.
4	IDNF(ID Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT (AboRTed command)	This bit is set if the command has been aborted because of the card status condition.(Not ready. Write fault, Invalid command, etc.)
0	AMNF (Address Mark Not Found	This bit is set in case of a general error.

3. Feature register

This register is write-only register, and provides information regarding features of the drive that the host wishes to utilize.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature byte							

4. Sector count register

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. IF the value of this register is zero, a count of 256 sectors is specified. In plural sector transfer, if not successfully completed, the register contains the number of sectors, which need to be transferred in order to complete, the request.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector count byte							

5. Sector number register

This register contains the starting sector number, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector number byte							

6. Cylinder low register

This register contains the low 8-bit of the starting cylinder address, which is started by following sectors transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder low byte							

7. Cylinder high register

This register contains the high 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder high byte							

8. Drive head register

This register is used for selecting the Drive number and Head number for the following command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Obsolete	LBA	Obsolete	DRV	Head number			

bit	Name	Function
7	Obsolete	This bit is normally set to “1”
6	LBA	LBA IS A FLAG TO SELECT EITHER Cylinder/Head/Sector (CHS) or Logical Block Address (LBA) mode. When LBA =0. CHS mode is selected. When LBA=1.LBA mode is selected. In LBA MODE. The logical Block Address is interrupted as follows: LBA07~LBA00: Sector Number Register D7 to D0. LBA15~LBA08: Cylinder Low Register D7 to D0. LBA23~LBA16: Cylinder High Register D7 to D0. LBA27~LBA24: Drive / Head Register bits HS3 to HS0.
5	Obsolete	This bit is normally set to “1”.
4	DRV (Drive select)	This bit is used for selecting the Master (Card 0) and Slave (Card 1) in Master/Slave organization. The card is set to be Card 0 or 1 by using DRV# of the Socket and Copy register.
3	Head number	This bit is used for selecting the Head number for the following command. Bit 3 is MSB.

9. Status register

This register is read only register, and it indicates the card status of command execution. When this register is read in configured I/O card mode (INDEX=1,2,3) and level interrupt mode, -IREQ is negated.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

Bit	Name	Function
7	BSY (BuSY)	This bit is set when the card internal operation is execting. When this bit is set to “1”, other bits in this register are invalid.
6	DRDY (Drive ReaDY)	If this bit and DSC bit are set to “1”, the cards is capable of receiving the read or writes or seek requests. If this bit is set to”0”, the card prohibits these requests.
5	DWF (Drive Write Fault)	This bit is set if this card indicates the write fault status.
4	DSC (Drive Seek Complete)	This bit is set when the drive seeks complete.
3	DRQ (Data ReQuest)	This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the card receives the other command.
2	CORR (CORRected data)	This bit is set when a correctable data error has been occurred and the data has been corrected.
1	IDX (InDex)	This bit is always set to “0”
0	ERR (ERRor)	This bit is set when the previous command has ended is some type of error. The error information is set in the error register. This bist is cleared by the next command.

10. Alternate status register

This register is the same as Status register in physically, so the bit assignment refers to previous item of Status register. But this register is different from Status register that –IREQ is not negated when data read.

11. Command register

This register is write only register, and it is used for writing the command to execute the requested operation. The command codes is written in the command register, after the parameter is written is the Task File when the Compact Flash card is in Ready state.

Command	Command code	Used parameter						
		FR	SC	SN	CY	DR	HD	LBA
Check power mode	E5H or 98H	N	N	N	N	Y	N	N
Execute drive diagnostic	90H	N	N	N	N	Y	N	N
Erase sector	C0H	N	Y	Y	Y	Y	Y	Y
Format track	50H	N	Y	N	Y	Y	Y	Y
Identify Drive	ECH	N	N	N	N	Y	N	N
Idle	E3H or 97H	N	Y	N	N	Y	N	N
Idle immediate	E1h or 95h	N	N	N	N	Y	N	N
Initialize drive parameters	91H	N	Y	N	N	Y	Y	N
Read buffer	E4H	N	N	N	N	Y	N	N
Read multiple	C4H	N	Y	Y	Y	Y	Y	Y
Read long sector	22H or 23H	N	N	Y	Y	Y	Y	Y
Read sector	20H or 21H	N	Y	Y	Y	Y	Y	Y
Read verify sector	40h or 41h	N	Y	Y	Y	Y	Y	Y
Recalibrate	1Xh	N	N	N	N	Y	N	N
Request sense	03H	N	N	N	N	Y	N	N
Seek	7XH	N	N	Y	Y	Y	Y	Y
Set features	EFH	Y	N	N	N	Y	N	N
Set multiple mode	C6H	N	Y	N	N	Y	N	N
Set sleep mode	E6h or 99h	N	N	N	N	Y	N	N
Stand by	E2h or 96h	N	N	N	N	Y	N	N

Stand by immediate	E0h or 94h	N	N	N	N	Y	N	N
Translate sector	87H	N	Y	Y	Y	Y	Y	Y
Wear level	F5H	N	N	N	N	Y	Y	N
Write buffer	E8H	N	N	N	N	Y	N	N
Write long sector	32h or 33h	N	N	Y	Y	Y	Y	Y
Write multiple	C5H	N	Y	Y	Y	Y	Y	Y
Write multiple w/o erase	CDH	N	Y	Y	Y	Y	Y	Y
Write sector	30H or 31H	N	Y	Y	Y	Y	Y	Y
Write sector w/o erase	38H	N	Y	Y	Y	Y	Y	Y
Write verify	3CH	N	Y	Y	Y	Y	Y	Y

12 Device control register

This register is write only register and it is used for controlling the interrupt request and issuing an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	X	X	X	1	SRST nIEN	nIEN	0

bit	Name	Function
7 to 4	X	Don't care
3	1	This bit is set to "1"
2	SRST(Software ReSeT)	This bit is set to "1" in order to force the card to perform Task File Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to "0"
1	nIEN(Interrupt Enable)	This bit is used for enabling –IREQ. When this bit is set to "0", -IREQ is enabled. When this bit is set to "1", -IREQ is disabled.
0	0	This bit is set to "0".

13. Drive Address register

The register is read only register, and it is used for confirming the drive status. This register is provides for compatibility with the AT disk drive interface. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on bit7.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	nWTG	nHS3	nHS2	nH1	nHS0	nDS1	nDS0

bit	Name	Function
7	X	This bit remains tri-state when host read access.
6	nWTG (WriTing Gate)	This bit is set as 0
5 to2	nHS3 to Nhs0 (Head Select3-0)	These bits are the negative value of Head Select bits (bit3 to 0) in Drive/Head register.
1	nDS1(Idrive Select1)	This bit is 0 when drive 1 is active and selected.
0	nDS0 (Idrive Select0)	This bit is 0 when drive 0 is active and selected.

3.4 ATA Command Set

The following table lists the ATA commands that are supported by the Firmware.

Table3: Compact Flash Storage Card Command Set

No	Command set	Code	FR	SC	SN	CY	DR	HD	LBA
1	Check power mode	E5H, 98H	—	—	—	—	Y	—	—
2	Execute drive diagnostic	90H	—	—	—	—	—	—	—
3	Erase sector(s)	C0H	—	Y	Y	Y	Y	Y	Y
4	Format track	50H	—	Y	—	Y	Y	Y	Y
5	Identify Device	ECH	—	—	—	—	Y	—	—
6	Idle	E3H, 97H	—	Y	—	—	Y	—	—
7	Idle immediate	E1H, 95H	—	—	—	—	Y	—	—
8	Initialize drive parameters	91H	—	Y	—	—	Y	Y	—
9	Read buffer	E4H	—	—	—	—	Y	—	—
10	Read multiple	C4H	—	Y	Y	Y	Y	Y	Y
11	Read long	22H, 23H	—	—	Y	Y	Y	Y	Y
12	Read sector(s)	20H, 21H	—	Y	Y	Y	Y	Y	Y
13	Read verify sector(s)	40H, 41H	—	Y	Y	Y	Y	Y	Y
14	Recalibrate	1XH	—	—	—	—	Y	—	—
15	Request sense	03H	—	—	—	—	Y	—	—
16	Seek	7XH	—	—	Y	Y	Y	Y	Y
17	Set features	EFH	Y	—	—	—	Y	—	—
18	Set multiple mode	C6H	—	Y	—	—	Y	—	—
19	Set sleep mode	E6H, 99H	—	—	—	—	Y	—	—
20	Stand by	E2H, 96H	—	—	—	—	Y	—	—
21	Stand by immediate	E0H, 94H	—	—	—	—	Y	—	—
22	Translate sector	87H	—	Y	Y	Y	Y	Y	Y
23	Wear level	F5H	—	—	—	—	Y	Y	—
24	Write buffer	E8H	—	—	—	—	Y	—	—
25	Write long	32H, 33H	—	—	Y	Y	Y	Y	Y
26	Write multiple	C5H	—	Y	Y	Y	Y	Y	Y
27	Write multiple w/o erase	CDH	—	Y	Y	Y	Y	Y	Y
28	Write sector(s)	30H, 31H	—	Y	Y	Y	Y	Y	Y
29	Write sector(s) w/o erase	38H	—	Y	Y	Y	Y	Y	Y
30	Write verify	3CH	—	Y	Y	Y	Y	Y	Y

Notes: FR: Feature Register

SC: Sector Count register (00H to FFH, 00H means 256 sectors)

SN: Sector Number register

CY: Cylinder Low/High register

DR: Drive bit of Drive/Head register

HD: Head No. (0 to 15) of Drive/Head register

Y: Used for the command

—: Not used for the command

Identify Device Information

Word address	Default value	Bytes	Data field type information
0	848AH (045AH)	2	General configuration bit-significant information ※1
1	01F3H	2	Default number of cylinders
2	0000H	2	Reserved
3	0004H	2	Default number of heads
4	0000H	2	Number of unformatted bytes per track
5	0200H	2	Number of unformatted bytes per sector
6	0020H	2	Default number of sectors per track
7	0000H	4	Number of sectors per card
8	F980H	4	Number of sectors per card
9	0000H	2	Reserved
10	4346H	2	Serial Number (20 ASCII characters)
11	3030H	2	Serial Number (20 ASCII characters)
12	3030H	2	Serial Number (20 ASCII characters)
13	3030H	2	Serial Number (20 ASCII characters)
14	3030H	2	Serial Number (20 ASCII characters)
15	2020H	2	Serial Number (20 ASCII characters)
16	2020H	2	Serial Number (20 ASCII characters)
17	2020H	2	Serial Number (20 ASCII characters)
18	2020H	2	Serial Number (20 ASCII characters)
19	2020H	2	Serial Number (20 ASCII characters)
20	0001H	2	Buffer type (single ported)
21	0001H	2	Buffer size in 512 byte increments
22	0004H	2	# ECC bytes passed on Read/Write Long Commands
23	3034H	2	Firmware revision (8 ASCII characters)
24	3146H	2	Firmware revision (8 ASCII characters)
25	4120H	2	Firmware revision (8 ASCII characters)
26	2020H	2	Firmware revision (8 ASCII characters)
27	466CH	2	Model Number (40 ASCII characters)
28	6173H	2	Model Number (40 ASCII characters)
29	6820H	2	Model Number (40 ASCII characters)
30	4361H	2	Model Number (40 ASCII characters)
31	7264H	2	Model Number (40 ASCII characters)
32	2020H	2	Model Number (40 ASCII characters)
33	2020H	2	Model Number (40 ASCII characters)
34	2020H	2	Model Number (40 ASCII characters)
35	2020H	2	Model Number (40 ASCII characters)
36	2020H	2	Model Number (40 ASCII characters)
37	2020H	2	Model Number (40 ASCII characters)
38	2020H	2	Model Number (40 ASCII characters)
39	2020H	2	Model Number (40 ASCII characters)
40	2020H	2	Model Number (40 ASCII characters)
41	2020H	2	Model Number (40 ASCII characters)

※1: 045AH is for fixed mode.

Word address	Default value	Bytes	Data field type information
42	2020H	2	Model Number (40 ASCII characters)
43	2020H	2	Model Number (40 ASCII characters)
44	2020H	2	Model Number (40 ASCII characters)
45	2020H	2	Model Number (40 ASCII characters)
46	2020H	2	Model Number (40 ASCII characters)
47	0001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0A00H	2	Capabilities: DMA not Supported, LBA supported
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode 2
52	0000H	2	DMA data transfer cycle timing mode not Supported
53	0003H	2	Data Fields 54 to 58 are valid
54	01F3H	2	Number of current logical cylinders
55	0004H	2	Number of current logical heads
56	0020H	2	Number of current logical sectors per track
57	F980H	2	Current Capacity in sectors
58	0000H	2	Current Capacity in sectors
59	0100H	2	Multiple sector setting is valid
60	F980H	2	Total number of sectors addressable in LBA Mode
61	0000H	2	Total number of sectors addressable in LBA Mode
62 - 64	0000H	6	Reserved
65	XXXXH	2	Minimum Multiword DMA transfer cycle time per word. In PCMCIA mode this value shall be 0h
66	XXXXH	2	Recommended Multiword DMA transfer cycle time . In PCMCIA mode this value shall be 0h
67	XXXXH	2	Minimum PIO transfer cycle time without flow control
68	0078H	2	Minimum PIO transfer cycle time without flow control
69	0078H	2	Minimum PIO transfer cycle time with IORDY flow control
70 - 129	0000H	120	Reserved
130	3034H	2	Firmware version, string “04”
131	3035H	2	Firmware version, string “05”
132	3036H	2	Firmware version, string “06”
133	6238H	2	Firmware version, string “b8”
134 - 255	0000H	2	Reserved

3.5. DC Power Specification
3.5.1 Absolute Ratings

Symbol	Parameter	Ratings	Units
VDD	Supply voltage	- 0.3 to +7.0	V
VIN	Input Voltage	-0.3 to VDD +0.3	V
IIN	DC Input Current	-10	mA

3.5.2 Recommend operating conditions

Symbol	Parameter		Ratings	Units
VDD	DC supply voltage	5V	4.5 to +5.5	V
		3.3V	3.0 to +3.6	V

3.5.3 DC Characteristics 1(Vcc = 3.3V +/- 5%)

Symbol	Parameter		Conditions	MIN	TYP	MAX	Unix
VIH	High level input voltage	CMOS		2.0			V
VIL	Low level input voltage	CMOS				1.0	V
VT	Switching threshold	CMOS			1.4		V
VT+	Switching trigger , positive-going threshold	CMOS				2.0	V
VT-	Switching trigger , negative-going threshold	CMOS		1.0			V
IIH	High level input current	Input buffer	VIN = VDD	-10		10	uA
		Input buffer with pull-up		10	30	60	
IIL	Low level input current	Input buffer	VIN = VSS	-10		10	uA
		Input buffer with pull-up		-160	-30	-10	
VOH	High level output voltage	Type 4	IOH = -4 mA	2.4			V
		Type 4	IOH = -8 mA				
		Type 4	IOH = -16 mA				
VOL	Low level output voltage	Type 4	IOL = 4 mA			0.4	V
		Type 4	IOL = 8 mA				
		Type 4	IOL = 16 mA				
IOZ	Tri-state output leakage current		Vout = Vss or VDD	-10		10	uA
IDD	Maximum operating current (RMS)		VDD = 3.3 V fmclk = 30MHz		30	40	mA
Ipeak	Peak current					60	mA
Iidle	Idle current					10	mA
Ids	Stop current					300	uA

3.5.4 DC Characteristics 2 (Vcc = 5.0V +/- 10%)

Symbol	Parameter		Conditions	MIN	TYP	MAX	Unix
VIH	High level input voltage	CMOS		3.5			V
VIL	Low level input voltage	CMOS				1.5	V
VT	Switching threshold	CMOS			2.5		V
VT+	Switching trigger , positive-going threshold	CMOS				4.0	V
VT-	Switching trigger , negative-going threshold	CMOS		1.0			V
IIH	High level input current	Input buffer	VIN = VDD	-10		10	uA
		Input buffer with pull-up		10	50	100	
IIL	Low level input current	Input buffer	VIN = VSS	-10		10	uA

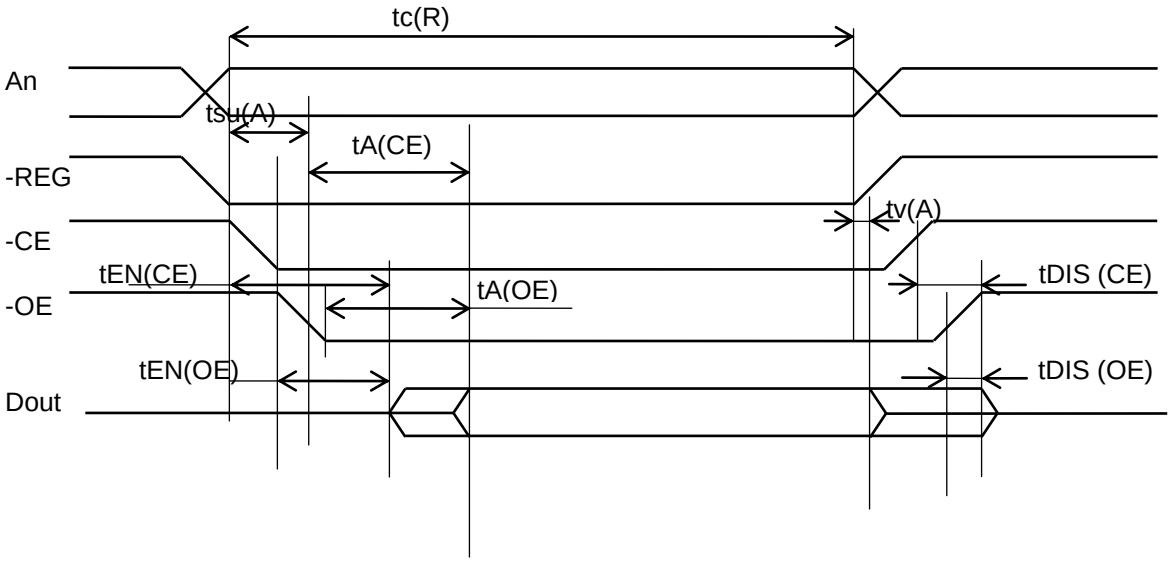
		Input buffer with pull-up		-100	-50	-10	
VOH	High level output voltage	Type 4	IOH = -4 mA	2.4			V
		Type 4	IOH = -8 mA				
		Type 4	IOH = -16 mA				
VOL	Low level output voltage	Type 4	IOL = 4 mA			0.4	V
		Type 4	IOL = 8 mA				
		Type 4	IOL = 16 mA				
IOZ	Tri-state output leakage current		Vout = Vss or VDD	-10		10	uA
IDD	Maximum operating current (RMS)		VDD = 5.0 V fmclk = 30MHz		30	40	mA
Ipeak	Peak current					60	mA
Iidle	Idle current					10	mA
Ids	Stop current					400	uA

3.6. AC Power characteristic

3.6.1 Attribute Memory Read AC Characteristics

SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	NOTES
tCR	Read cycle time	250	–	–	ns	
tA (A)	Address access time	–	250	–		
tA (CE)	-CE access time	–	250	–		
tA (OE)	-OE access time	–	125	–		
tDIS (CE)	Output disable time (-CE)	–	100	–		
tDIS (OE)	Output disable time (-OE)	–	100	–		
tEN (CE)	Output enable time (-CE)	5	–	–		
tEN (OE)	Output enable time (-OE)	5	–	–		
tV (A)	Data valid time (A)	0	–	–		
tSU (A)	Address setup time	30	–	–		

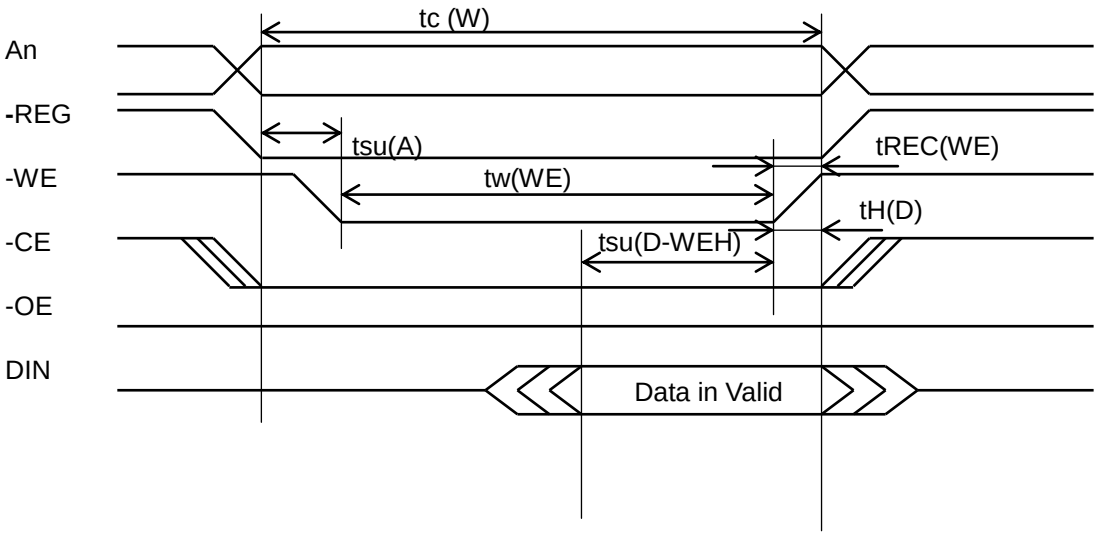
Attribute Memory Read Timing



3.6.2 Attribute Memory Write Timing

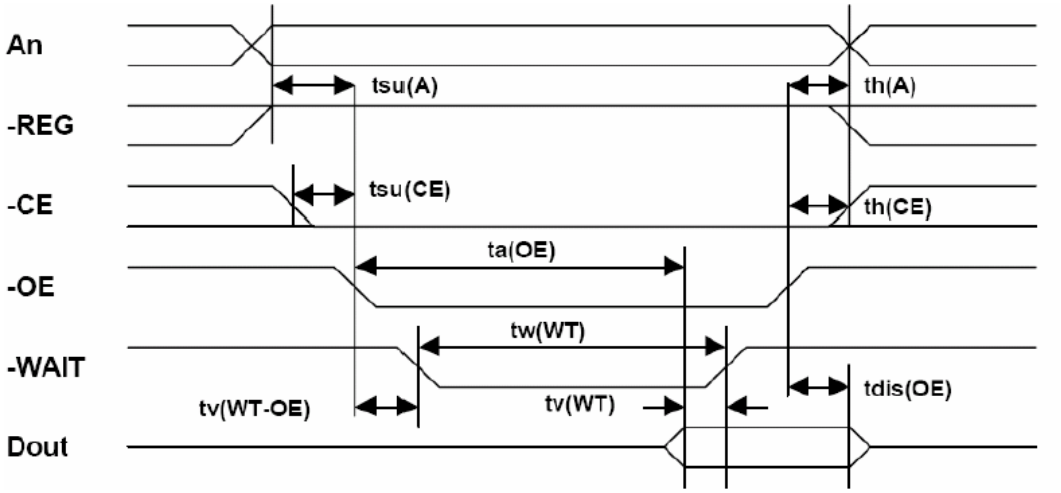
SYMBOL	PARAMETER	MIN	MAX	TYP	UNIT	NOTES
tCW	Write cycle time	250	–	–	ns	
tW (WE)	Write pulse time	150	–	–		
tSU (A)	Access setup time	30	–	–		
tSU (D-WEH)	Data setup time (-WE)	30	–	–		
tH (D)	Data hold time	30	–	–		
tREC (WE)	Write recover time	30	–	–		

Attribute Memory Write Timing



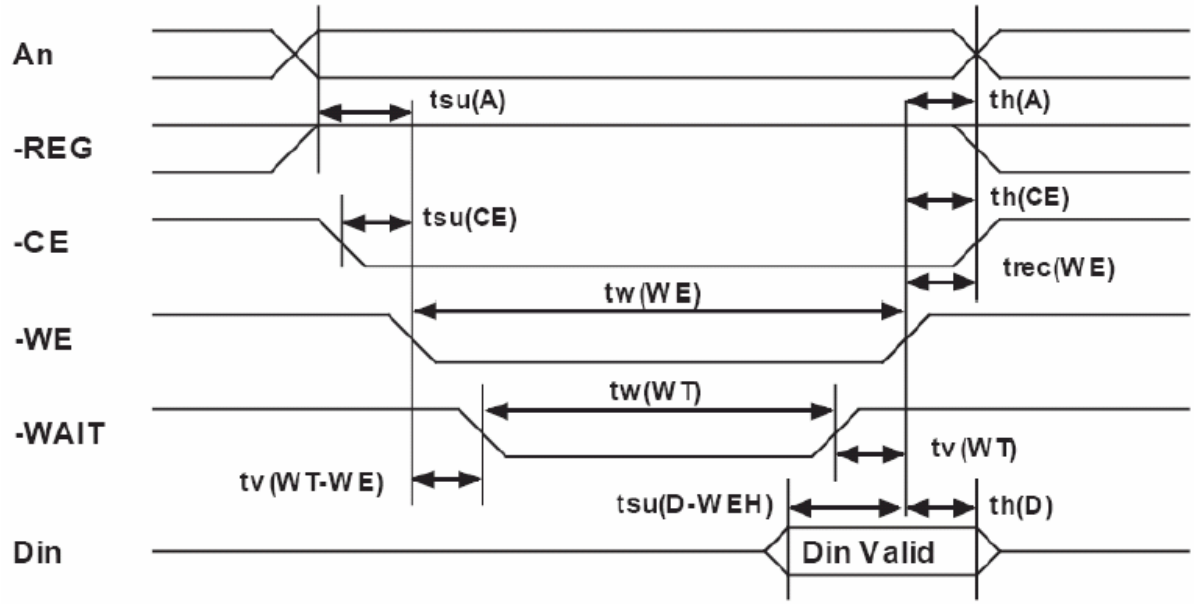
3.6.3 Common Memory Read Timing Specification

SYMBOL	PARAMETER	MIN	MAX	UNIT
ta (OE)	-OE access time		125	ns
tdis (OE)	Output disable time (-OE)		100	
tSU (A)	Address setup time	30		
th (A)	Address Hold time	20		
tSU (CE)	CE setup before OE	0		
th (CE)	CE Hold following OE	20		
tv (WT-OE)	Wait Delay Falling from OE		35	
tv (WT)	Data Setup for Wait Release		0	
tw (WT)	Wait Width Time		350	



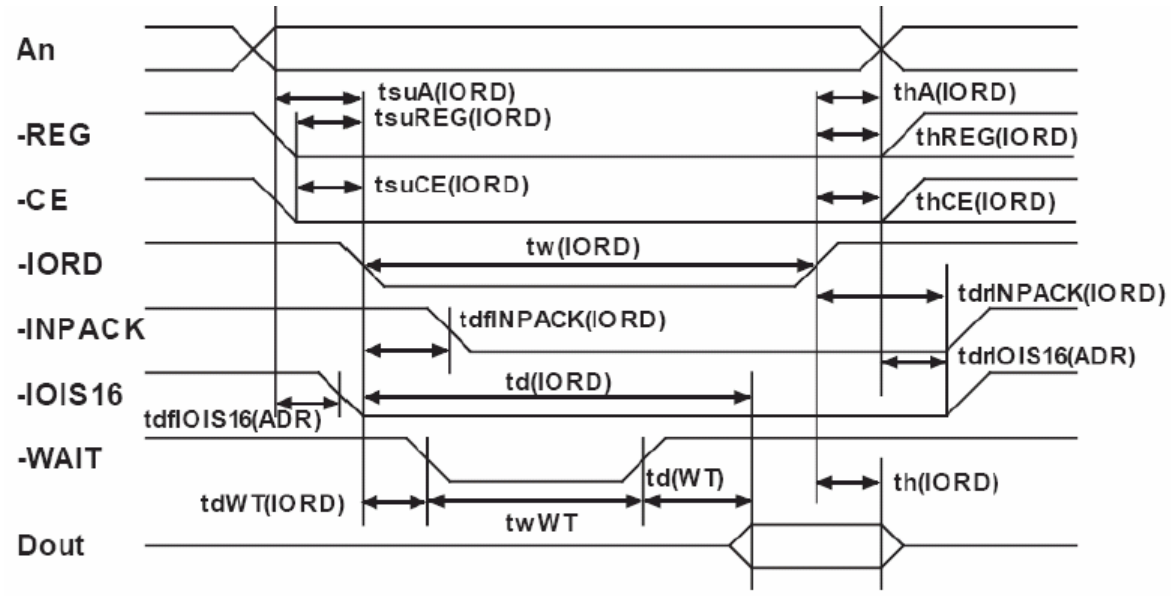
3.6.4 Common Memory Write Timing Specification

SYMBOL	PARAMETER	MIN	MAX	UNIT
tSU (D-WEH)	Data Setup before WE	80		ns
th (D)	Data Hold following WE	30		
tw (WE)	WE Pulse Width	150		
tSU (A)	Address setup Time	30		
tSU (CE)	CE Setup before WE	0		
trec (WE)	Write Recovery Time	30		
th (A)	Address Hold Time	20		
th (CE)	CE Hold following WE	20		
tv (WT-WE)	Wait Delay Falling from WE		35	
tv (WT)	WE High from Wait Release	0		
tw (WT)	Wait Width Time		350	



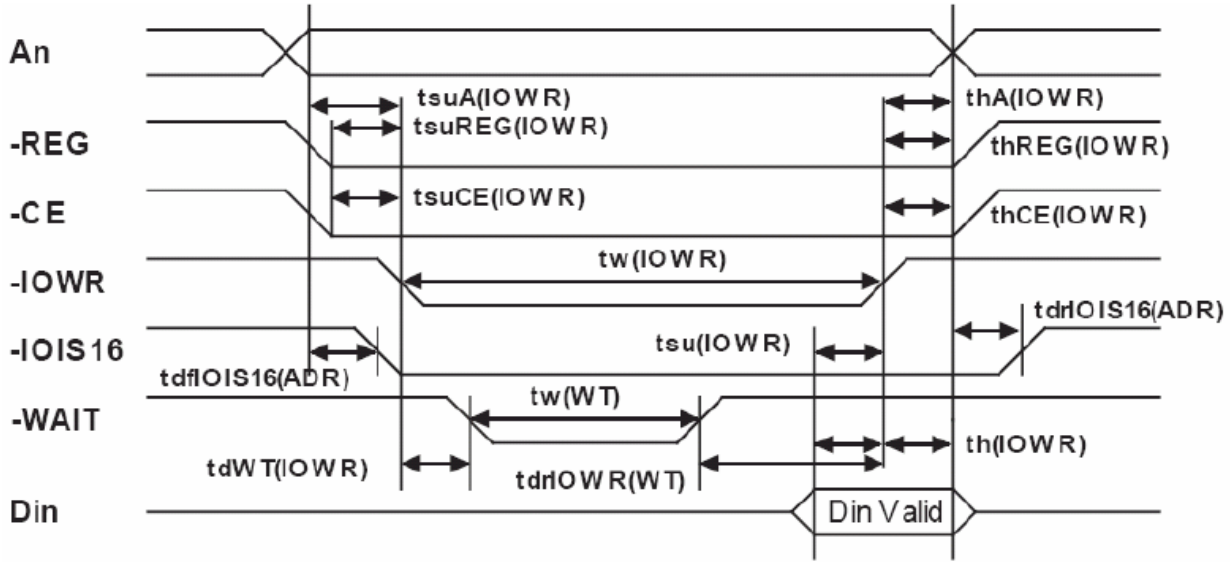
3.6.5 I/O Output (Read) Timing Specification

SYMBOL	PARAMETER	MIN	MAX	UNIT
td (IORD)	Data Delay after IORD		100	ns
th (IORD)	Data Hold following WE	0		
tw (IORD)	WE Pulse Width	165		
tSUA (IORD)	Address setup before IORD	70		
thA (IORD)	Address Hold following IORD	20		
tSUCE (IORD)	CE Setup before IORD	5		
thCE (IORD)	CE Hold following IORD	20		
tSUREG (IORD)	REG Setup before IORD	5		
thREG (IORD)	REG Hold following IORD	0		
tdfINPACK (IORD)	INPACK Delay Falling from IORD	0	45	
tdrINPACK (IORD)	INPACK Delay Rising from IORD		45	
tdfIOIS16 (IORD)	IOIS16 Delay Falling from Address		35	
tdrIOIS16 (IORD)	IOIS16 Delay Rising from Address		35	
tdWT (IORD)	Wait Delay Falling from IORD		35	
td (WT)	Data Delay from Wait Rising		0	
tw (WT)	Wait Width Time		350	

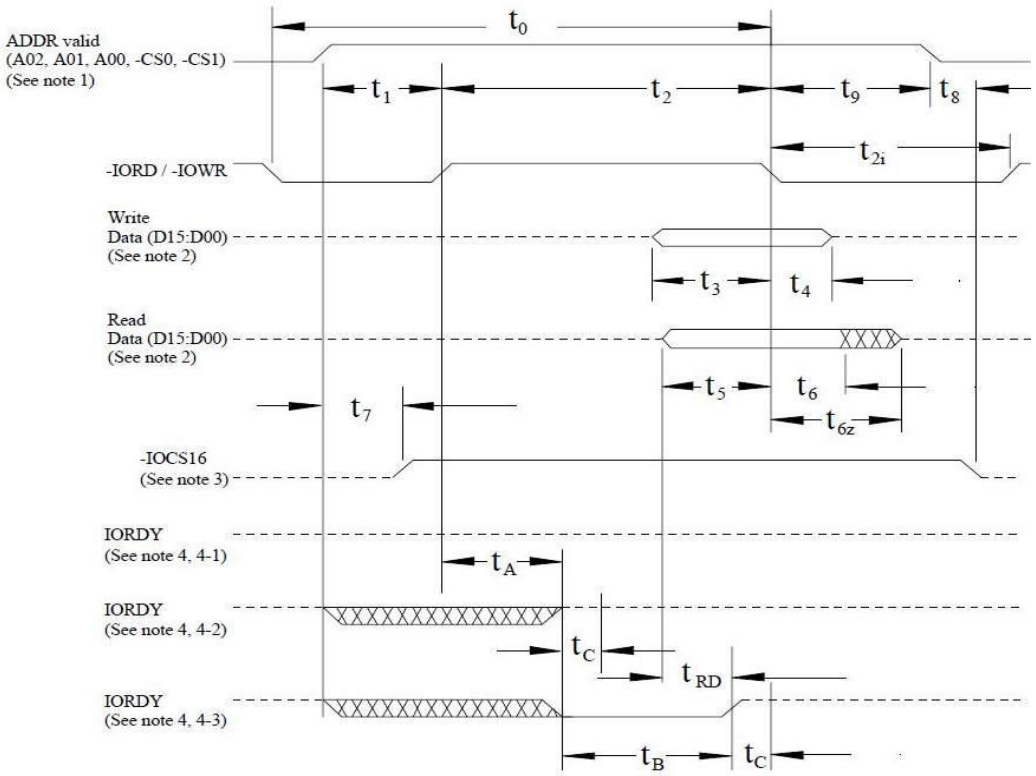


3.6.6 I/O Input (Write) Timing Specification

SYMBOL	PARAMETER	MIN	MAX	UNIT
tsu (IOWR)	Data Delay before IOWR	60		ns
th (IOWR)	Data Hold following IOWR	30		
tw (IOWR)	IOWR Width Time	165		
tSUA (IOWR)	Address setup before IOWR	70		
thA (IOWR)	Address Hold following IOWR	20		
tSUCE (IOWR)	CE Setup before IOWR	5		
thCE (IOWR)	CE Hold following IOWR	20		
tSUREG (IOWR)	REG Setup before IOWR	5		
thREG (IOWR)	REG Hold following IOWR	0		
TdfIOIS16 (ADR)	IOIS16 Delay Falling from Address		35	
TdrIOIS16 (ADR)	IOIS16 Delay Rising from Address		35	
tdWT (IOWR)	Wait Delay Falling from IOWR		35	
tdrIOWR (WT)	IOWR high from Wait high	0		
tw (WT)	Wait Width Time		350	



3.6.7 True IDE Mode PIO Read/Write Timing
(AC46series supports only PIO mode 4)



Notes:
(1) Device address consists of -CS0, -CS1, and A[02::00]
(2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
(3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
(4-1) Device never negates IORDY: No wait is generated.
(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

True IDE Mode I/O Read/Write Timing

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	Note
t0	Cycle time (min)	600	383	240	180	120	1
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	
t2	-IORD/-IOWR (min)	165	125	100	80	70	1
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	1
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	1
t3	-IOWR data setup (min)	60	45	30	30	20	
t4	-IOWR data hold (min)	30	20	15	10	10	
t5	-IORD data setup (min)	50	35	20	20	20	
t6	-IORD data hold (min)	5	5	5	5	5	
t6Z	-IORD data tristate (max)	30	30	30	30	30	2
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	4
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	4
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	
tRD	Read Data Valid to IORDY active (min). If IORDY initially low after tA	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	
tC	IORDY assertion to release (max)	5	5	5	5	5	

Notes:

The maximum load on -IOCS16 is 1 LSTTL with a 50 pF total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width must still be met.

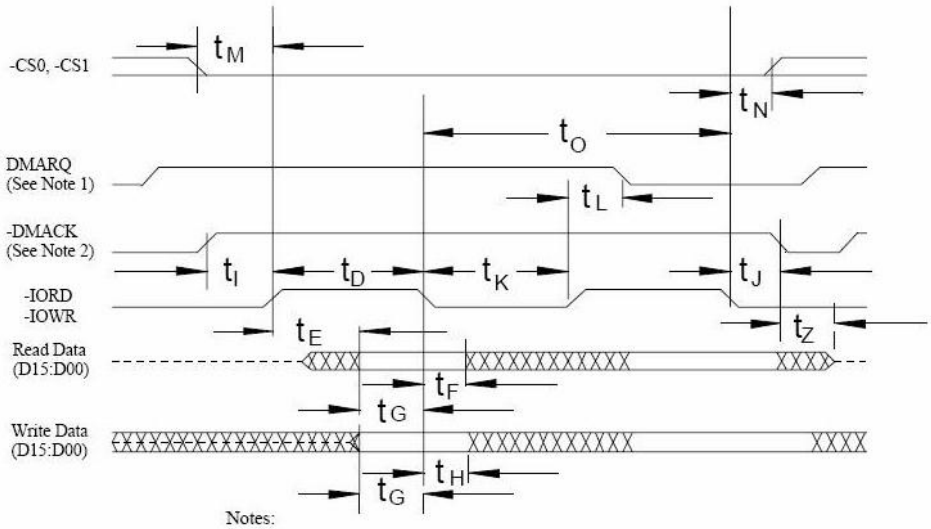
(1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify drive data. A CompactFlash Storage Card implementation shall support any legal host implementation.

(2) This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).

(3) The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the CompactFlash Storage Card is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.

(4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.

3.6.8 True IDE mode Multiword DMA Read/Write Timing
(AC46series supports only Multiword DMA mode 2)



Notes:

(1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.

(2) This signal may be negated by the host to suspend the DMA transfer in progress.

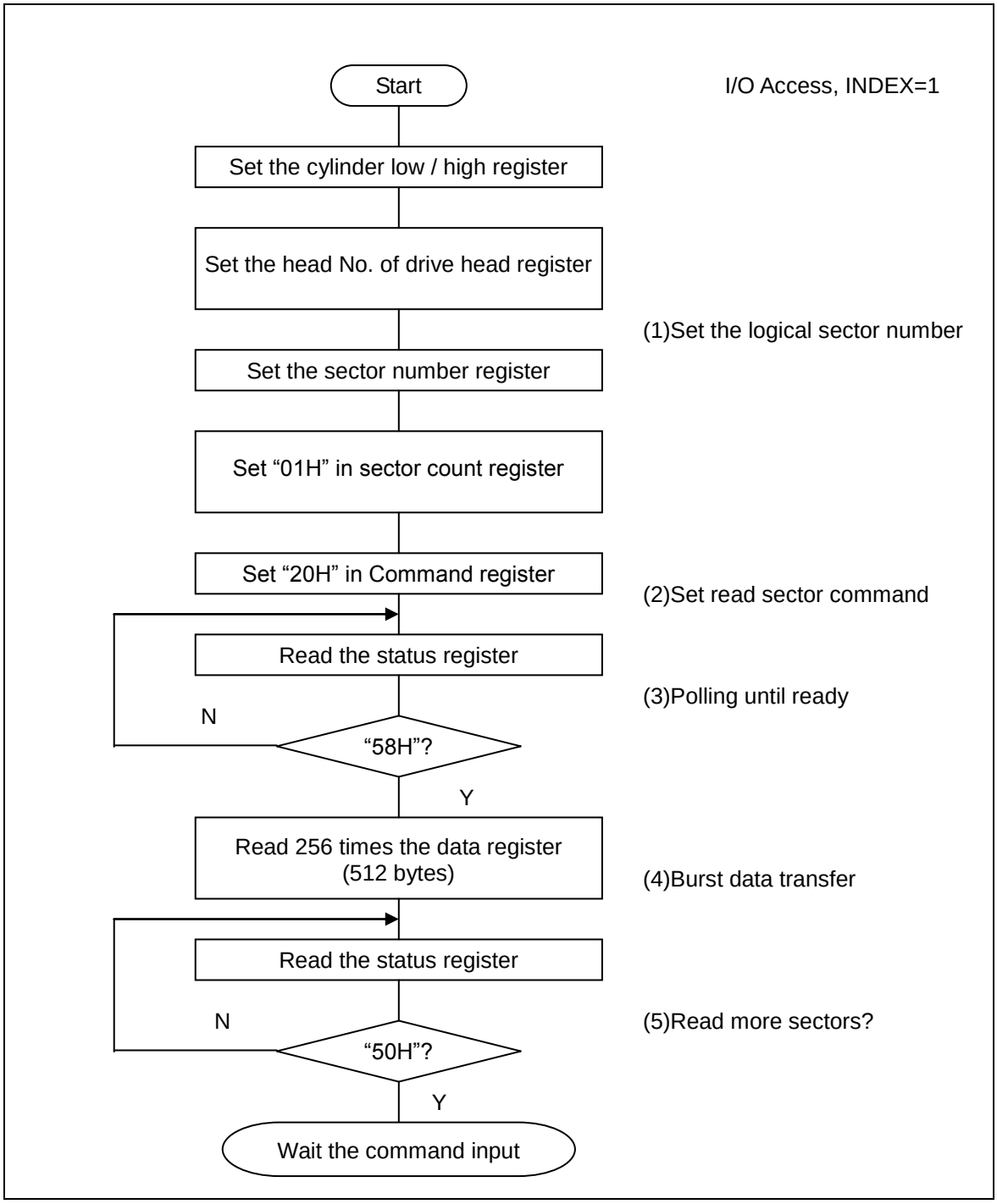
True IDE Multiword DMA Mode Read/Write Timing

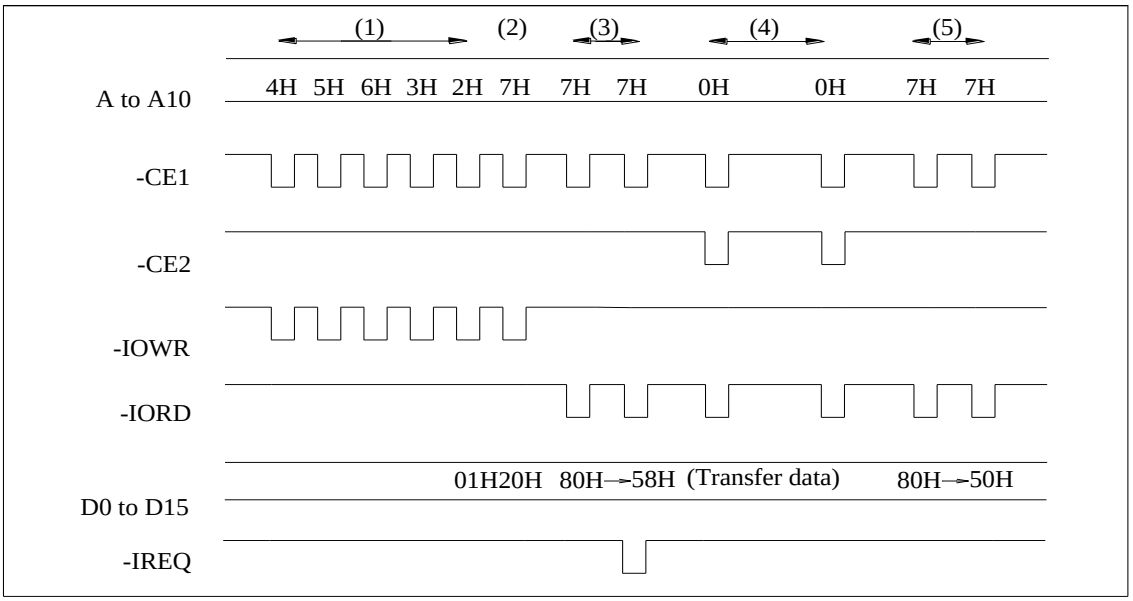
	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	Note
t_O	Cycle time (min)	480	150	120	100	80	1
t_D	-IORD / -IOWR asserted width (min)	215	80	70	65	55	1
t_E	-IORD data access (max)	150	60	50	50	45	
t_F	-IORD data hold (min)	5	5	5	5	5	
t_G	-IORD/-IOWR data setup (min)	100	30	20	15	10	
t_H	-IOWR data hold (min)	20	15	10	5	5	
t_I	DMACK to –IORD/-IOWR setup (min)	0	0	0	0	0	
t_J	-IORD / -IOWR to -DMACK hold (min)	20	5	5	5	5	
t_{KR}	-IORD negated width (min)	50	50	25	25	20	1
t_{KW}	-IOWR negated width (min)	215	50	25	25	20	1
t_{LR}	-IORD to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	35	35	
t_M	CS(1:0) valid to –IORD / -IOWR	50	30	25	10	5	
t_N	CS(1:0) hold	15	10	10	10	10	
t_Z	-DMACK	20	25	25	25	25	

Notes: 1) t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_{KR}, and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR} or t_{KW} for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR}, and t_{KW} as needed to ensure that t_0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

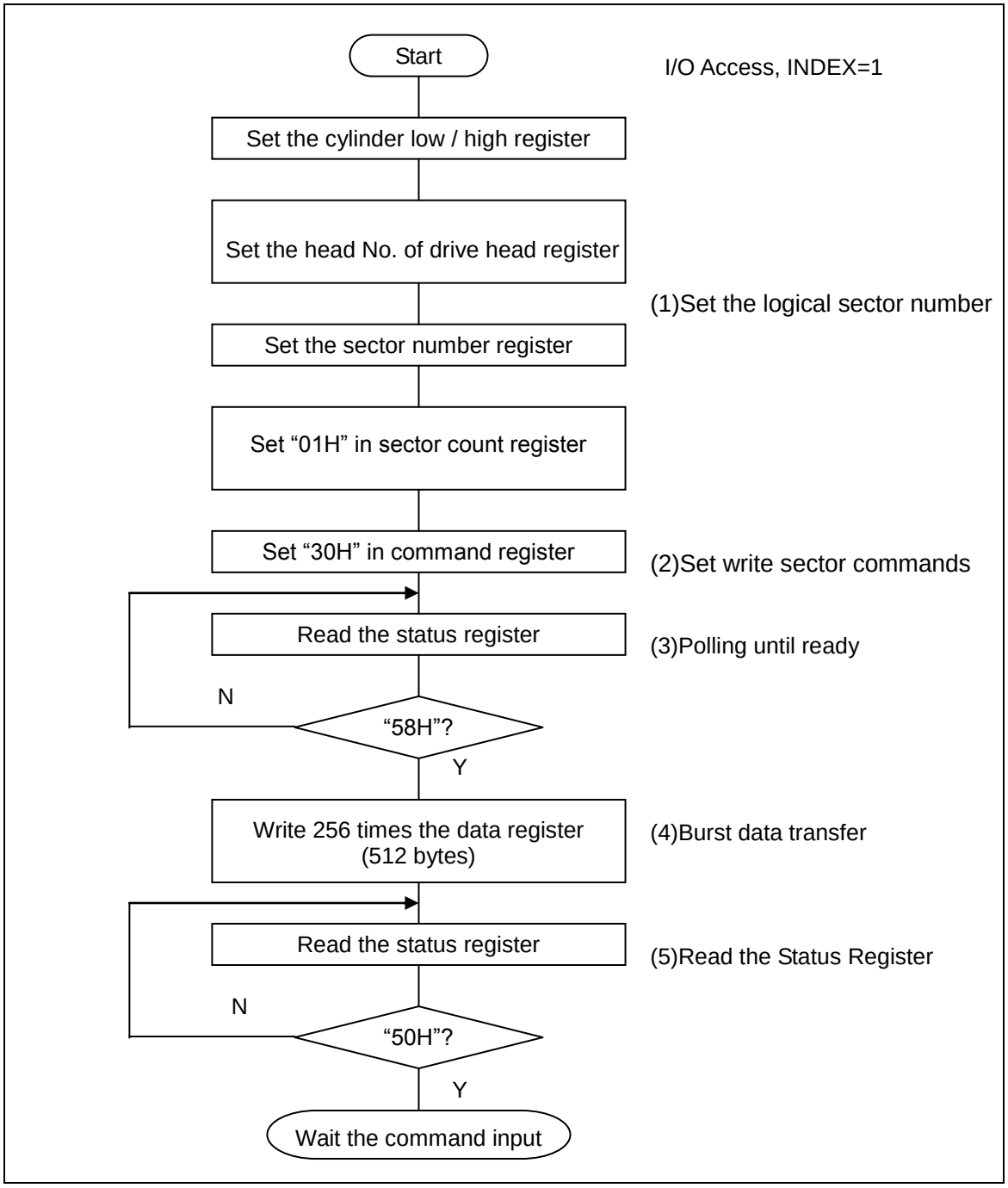
3.7 Sector Transfer Protocol

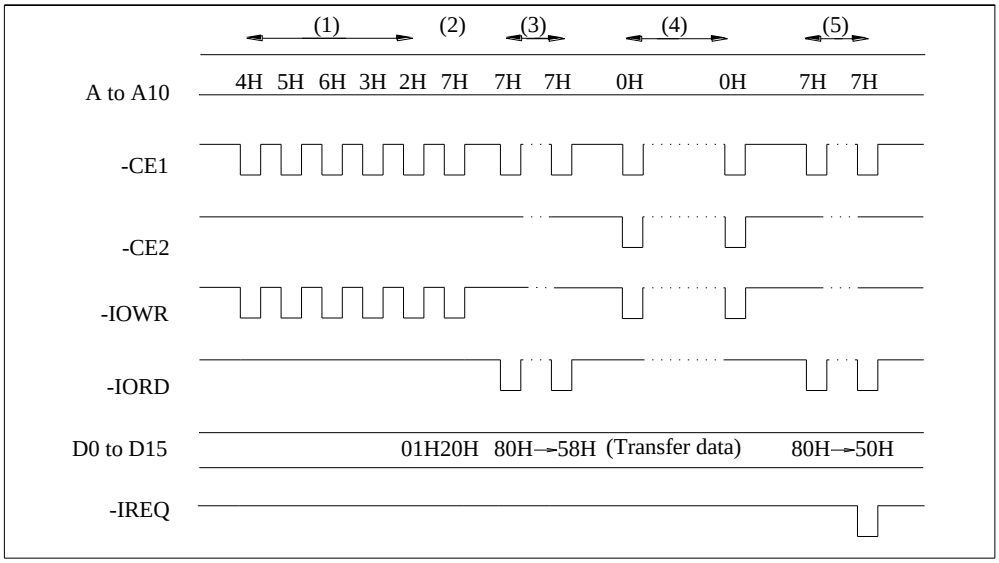
Sector read: 1 sector read procedure after the card configured I/O interface is shown as follows.




(1)
(2)
(3)
(4)
(5)
A to A10
4H 5H 6H 3H 2H 7H 7H 7H 0H 0H 7H 7H
-CE1
-CE2
-IOWR
-IORD
D0 to D15
01H 20H 80H→58H (Transfer data) 80H→50H
-IREQ

Sector write: 1 sector write procedure after the card configured I/O interface is shown as follows.




(1)
(2)
(3)
(4)
(5)
A to A10
4H 5H 6H 3H 2H 7H 7H 7H 0H 0H 7H 7H
-CE1
-CE2
-IOWR
-IORD
D0 to D15
01H20H 80H→58H (Transfer data) 80H→50H
-IREQ