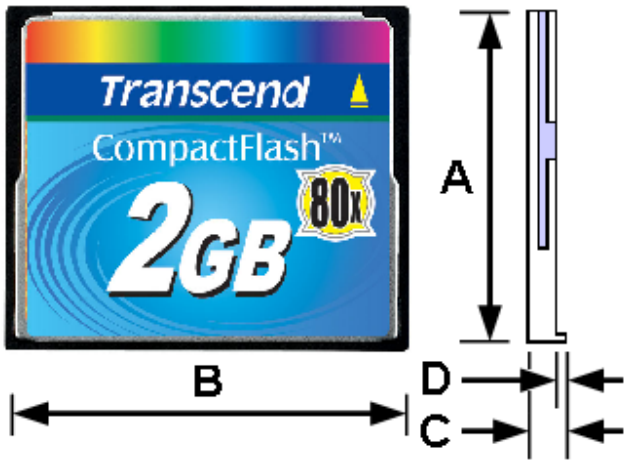
Description

The Transcend CF 80X is a High Speed Compact Flash Card with high quality Flash Memory assembled on a printed circuit board.

Placement



Features

- RoHS compliant products
- Compliant with CompactFlash® specification V3.0
- Single Power Supply: 5V, 3.3V
- Compliant to CompactFlash, PCMCIA, and ATA standards
- Support PIO mode 0 to PIO mode 6
- Support Multi-Word DMA mode 0 to Multi-Word DMA mode 4 (Series of –NR and –NF don't support Multi-Word DMA mode, please see Ordering Information)
- Operating Temperature: 0°C to 70°C
- Storage Temperature: -25°C to 85°C
- Hardware RS-code ECC
- Flash Interface: Dual Channel 8-bit access
  Single Channel 16-bit access
- Endurance: 1,000,000 Program/Erase cycles
- Durability of Connector: 10,000 times
- MTBF: 1,000,000 hours

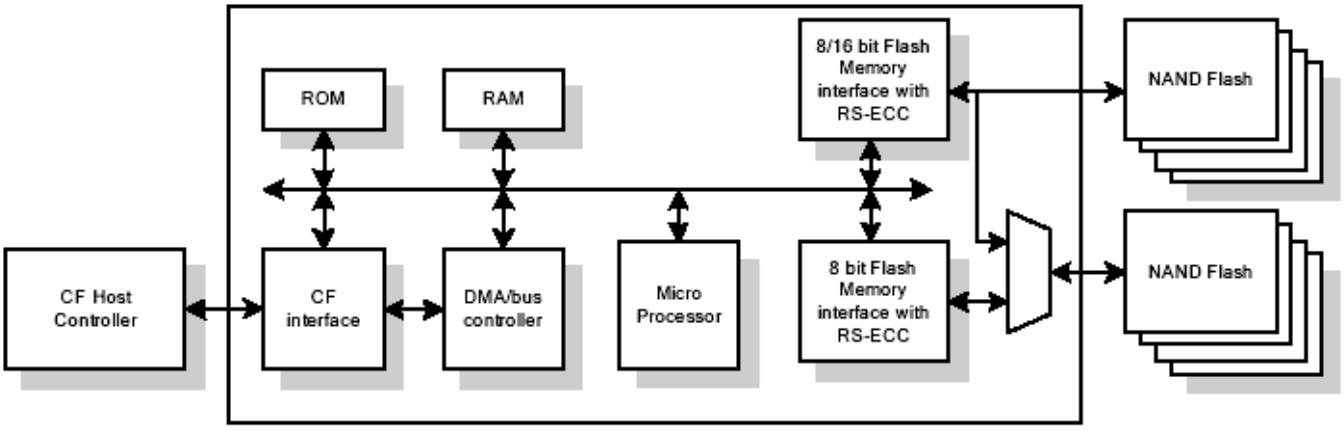
Dimensions

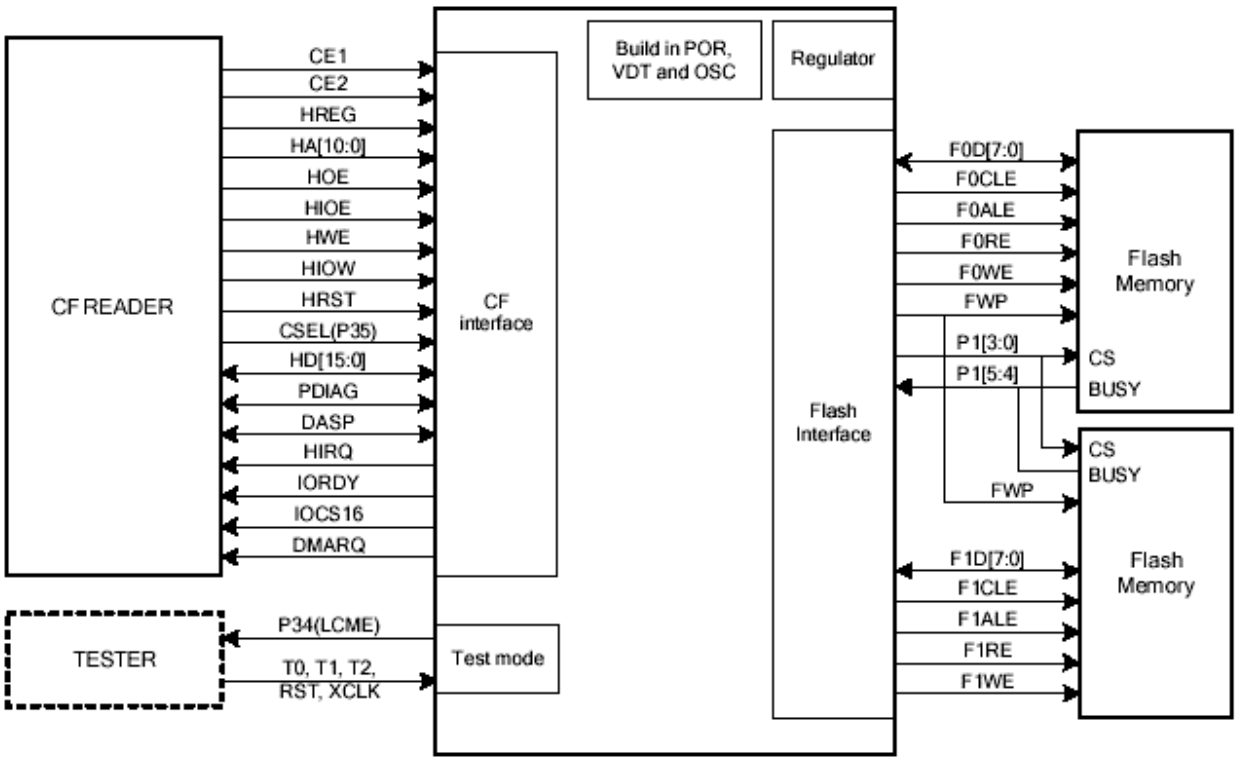
Side	Millimeters	Inches
A	36.40 ± 0.150	1.43 ± 0.005
B	42.80 ± 0.100	1.69 ± 0.004
C	3.30 ± 0.100	0.13 ± 0.004
D	0.63 ± 0.070	0.02 ± 0.003

Ordering Information

	Part Number	Description
CF80	TS32M~2GCF80	DMA Removable
	TS32M~2GCF80-DF	DMA Fixed Disk
	TS32M~2GCF80-NR	Non-DMA Removable
	TS32M~2GCF80-NF	Non-DMA Fixed Disk

Block Diagram





Pin Function Description

Flash Interface

Pin Name	Direction	Description
F0D[7:0]	I/O	8 bit : Flash0 interface data bus, direct connect to the flash memory. 16 bit : Flash interface data bus low byte, direct connect to the flash memory.
F0CLE	O	Flash0 interface command latch enable, direct connect to the flash memory.
F0ALE	O	Flash0 interface address latch enable, direct connect to the flash memory.
F0RE	O	Flash0 interface read strobe control, direct connect to the flash memory.
F0WE	O	Flash0 interface write strobe control, direct connect to the flash memory.
F1D[7:0]	I/O	8 bit : Flash1 interface data bus, direct connect to the flash memory. 16 bit : Flash interface data bus high byte, direct connect to the flash memory.
F1CLE	O	8 bit : Flash1 interface command latch enable, direct connect to the flash memory. 16 bit : NC
F1ALE	O	8 bit : Flash1 interface address latch enable, direct connect to the flash memory. 16 bit : NC
F1RE	O	8 bit : Flash1 interface read strobe control, direct connect to the flash memory. 16 bit : NC
F1WE	O	8 bit : Flash1 interface write strobe control, direct connect to the flash memory. 16 bit : NC
FWP	O	Flash interface write protection, direct connect to the flash memory.
P1[3:0]	O	Used as flash chip select signal.
P1[5:4]	I	Used as busy signal from flash memory.
VCC3	Power in	Power supply for flash group I/O pad.

Test Pin

Pin Name	Direction	Description
T2	I	Test mode selection, tie to ***low*** for normal operation.
T1	I	Test mode selection, tie to ***low*** for normal operation.
T0	I	Test mode selection, tie to ***low*** for normal operation.
RST, XCLK	I	Reserved for CP/FT. tie to ***high*** for normal operation.
P34	I/O	Reserved for debug. ***floating*** for normal operation.
XROMA[14:0]	O	External ROM address line.
XROMD[7:0]	I	External ROM data line.
LDE	I	Reserved for debug, tie to ***low*** for normal operation.
XRAMOE	O	Reserved for debug, ***floating*** for normal operation.
XRAMWE	O	Reserved for debug, ***floating*** for normal operation.
XRAMCS	O	Reserved for debug, ***floating*** for normal operation.
XROME	I	Reserved for debug, tie to ***low*** for normal operation.

CompactFlash Interface

Pin Name	Direction	Description
CE1	I	CompactFlash interface chip select signal
CE2	I	CompactFlash interface chip select signal
HREG	I	CompactFlash interface control signal
HA[10:0]	I	CompactFlash interface address
HOE	I	CompactFlash interface output enable
HIOE	I	CompactFlash interface I/O output enable
HWE	I	CompactFlash interface write enable
HIOW	I	CompactFlash interface I/O write enable
CSEL(P35)	I	CompactFlash interface master/slaver control signal
HRST	I	CompactFlash interface reset signal
HD[15:0]	I/O	CompactFlash interface data bus
PDIAG	I/O	CompactFlash interface master/slaver handshake signal
DASP	I/O	CompactFlash interface master/slaver handshake signal
HIRQ	O	CompactFlash interface interrupt signal
IORDY	O	CompactFlash interface wait state signal
IOCS16	O	CompactFlash interface data bus width status
DMARQ	O	CompactFlash interface DMA request signal
VCC35	Power in	Power supply for CompactFlash interface group I/O pad.

System Configuration Pin

Pin Name	Direction	Description
P16	I	Reserved
P17	O	Hardware Pre-Test.

Voltage Regulator

Pin Name	Direction	Description
VD18	Power out	1.8V / 100 mA power supply.
VD33	Power in	Regulator in. Direct connect to card source power.
VSSA	Ground	Analog ground.

Other Power Pin

Pin Name	Direction	Description
VCCK	Power in	**CTL** kernel power supply. 1.8V input.
GND	Ground	Ground.

DC Character

CompactFlash interface I/O at 5.0V

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply Voltage	V_{CC}	4.5	5.5	V	
High level output voltage	V_{OH}	V_{CC}-0.8		V	
Low level output voltage	V_{OL}		0.8	V	
High level input voltage	V_{IH}	4.0		V	Non-schmitt trigger
		2.6	3.04	V	Schmitt trigger
Low level input voltage	V_{IL}		0.8	V	Non-schmitt trigger
		1.53	1.79	V	Schmitt trigger
Pull up resistance	R_{PU}	52.54.	86.56	kOhm	
Pull down resistance	R_{PD}	63	244	kOhm	

CompactFlash interface I/O at 3.3V

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply Voltage	V_{CC}	2.97	3.63	V	
High level output voltage	V_{OH}	V_{CC}-0.8		V	
Low level output voltage	V_{OL}		0.8	V	
High level input voltage	V_{IH}	2.4		V	Non-schmitt trigger
		1.67	1.88	V	Schmitt trigger
Low level input voltage	V_{IL}		0.6	V	Non-schmitt trigger
		0.92	1.07	V	Schmitt trigger
Pull up resistance	R_{PU}	81.39	154.85	kOhm	
Pull down resistance	R_{PD}	42	172	kOhm	

The other I/O

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply Voltage	V_{CC}	2.7	3.6	V	
High level output voltage	V_{OH}	2.4		V	
Low level output voltage	V_{OL}		0.4	V	
High level input voltage	V_{IH}	2.0		V	Non-schmitt trigger
		1.4	2.0	V	Schmitt trigger
Low level input voltage	V_{IL}		0.8	V	Non-schmitt trigger
		0.8	1.2	V	Schmitt trigger
Pull up resistance	R_{PU}	40		kOhm	
Pull down resistance	R_{PD}	40		kOhm	

AC Character

Attribute Memory Read Timing

Speed Version		300 ns	
Item	Symbol	Min ns.	Max ns.
Read Cycle Time	tc(R)	300	
Address Access Time	ta(HA)		300
Card Enable Access Time	ta(CEx)		300
Output Enable Access Time	ta(HOE)		150
Output Disable Time from CEx	tdis(CEx)		100
Output Disable Time from HOE	tdis(HOE)		100
Address Setup Time	tsu (HA)	30	
Output Enable Time from CEx	ten(CEx)	5	
Output Enable Time from HOE	ten(HOE)	5	
Data Valid from Address Change	tv(HA)	0	

Configuration Register (Attribute Memory) Write Timing

Speed Version		250 ns	
Item	Symbol	Min ns	Max ns
Write Cycle Time	tc(W)	250	
Write Pulse Width	tw(HWE)	150	
Address Setup Time	tsu(HA)	30	
Write Recovery Time	trec(HWE)	30	
Data Setup Time for HWE	tsu(HD-HWEH)	80	
Data Hold Time	th(HD)	30	

Common Memory Read Timing

Cycle Time Mode:		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Output Enable Access Time	ta(HOE)		125		60		50		45
Output Disable Time from	tdis(HOE)		100		60		50		45
Address Setup Time	tsu(HA)	30		15		10		10	
Address Hold Time	th(HA)	20		15		15		10	
CEx Setup before HOE	tsu(CEx)	0		0		0		0	
CEx Hold following HOE	th(CEx)	20		15		15		10	
Wait Delay Falling from HOE	tv(IORDY-HOE)		35		35		35		na
Data Setup for Wait Release	tv(IORDY)		0		0		0		na
Wait Width Time	tw(IORDY)		350		350		350		na

Common Memory Write Timing

Cycle Time Mode:		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before HWE	tsu (HD-HWEH)	80		50		40		30	
Data Hold following HWE	th(HD)	30		15		10		10	
HWE Pulse Width	tw(HWE)	150		70		60		55	
Address Setup Time	tsu(HA)	30		15		10		10	
CEx Setup before WE	tsu(CEx)	0		0		0		0	
Write Recovery Time	trec(HWE)	30		15		15		15	
Address Hold Time	th(HA)	20		15		15		15	
CEx Hold following HWE	th(CEx)	20		15		15		10	
Wait Delay Falling from HWE	tv (IORDY-HWE)		35		35		35		na
HWE High from Wait Release	tv(IORDY)	0		0		0		na	
Wait Width Time	tw (IORDY)		350		350		350		na

I/O Read Timing

Cycle Time Mode:		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Delay after HIOE	td(HIOE)		100		50		50		45
Data Hold following HIOE	th(HIOE)	0		5		5		5	
HIOE Width Time	tw(HIOE)	165		70		65		55	
Address Setup before HIOE	tsuHA(HIOE)	70		25		25		15	
Address Hold following HIOE	thHA(HIOE)	20		10		10		10	
CEx Setup before HIOE	tsuCEx(HIOE)	5		5		5		5	
CEx Hold following HIOE	thCEx(HIOE)	20		10		10		10	
HREG Setup before HIOE	tsuHREG (HIOE)	5		5		5		5	
HREG Hold following HIOE	thHREG (HIOE)	0		0		0		0	
Wait Delay Falling from HIOE	tdIORDY(HIOE)		35		35		35		na
Data Delay from Wait Rising	td(IORDY)		0		0		0		na
Wait Width Time	tw(IORDY)		350		350		350		na

I/O Write Timing

Cycle Time Mode:		255 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before HIOW	tsu(HIOW)	60		20		20		15	
Data Hold following HIOW	th(HIOW)	30		10		5		5	
HIOW Width Time	tw(HIOW)	165		70		65		55	
Address Setup before HIOW	tsuHA(HIOW)	70		25		25		15	
Address Hold following HIOW	thHA(HIOW)	20		20		10		10	
CEx Setup before HIOW	tsuCEx (HIOW)	5		5		5		5	
CEx Hold following HIOW	thCEx (HIOW)	20		20		10		10	
HREG Setup before HIOW	tsuHREG (HIOW)	5		5		5		5	
HREG Hold following HIOW	thHREG (HIOW)	0		0		0		0	
Wait Delay Falling from HIOW	tdIORDY(HIOW)		35		35		35		na
HIOW high from Wait high	tdrHIOW (IORDY)	0		0		0		na	
Wait Width Time	tw(IORDY)		350		350		350		na

True IDE PIO Mode Read/Write Timing

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
t0	Cycle time (min)	600	383	240	180	120	100	80
t1	Address Valid to HIOE/HIOW setup (min)	70	50	30	30	25	15	10
t2	HIOE/HIOW (min)	165	125	100	80	70	65	55
t2	HIOE/HIOW (min) Register (8 bit)	290	290	290	80	70	65	55
t2i	HIOE/HIOW recovery time (min)	-	-	-	70	25	25	20
t3	HIOW data setup (min)	60	45	30	30	20	20	15
t4	HIOW data hold (min)	30	20	15	10	10	5	5
t5	HIOE data setup (min)	50	35	20	20	20	15	10
t6	HIOE data hold (min)	5	5	5	5	5	5	5
t6Z	HIOE data tristate (max)	30	30	30	30	30	20	20
t7	Address valid to IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a
t8	Address valid to IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a
t9	HIOE/HIOW to address valid hold	20	15	10	10	10	10	10
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0
tA	IORDY Setup time	35	35	35	35	35	na	na
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na	na
tC	IORDY assertion to release (max)	5	5	5	5	5	na	na

True IDE Multiword DMA Mode Read/Write Timing

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	Note
tO	Cycle time (min)	480	150	120	100	80	1
tD	HIOE / HIOW asserted width (min)	215	80	70	65	55	1
tE	HIOE data access (max)	150	60	50	50	45	
tF	HIOE data hold (min)	5	5	5	5	5	
tG	HIOE/HIOW data setup (min)	100	30	20	15	10	
tH	HIOW data hold (min)	20	15	10	5	5	
tI	DMACK(HREG) to HIOE/HIOW setup (min)	0	0	0	0	0	
tJ	HIOE / HIOW to -DMACK hold (min)	20	5	5	5	5	
tKR	HIOE negated width (min)	50	50	25	25	20	1
tKW	HIOW negated width (min)	215	50	25	25	20	1
tLR	HIOE to DMARQ delay (max)	120	40	35	35	35	
tLW	HIOW to DMARQ delay (max)	40	40	35	35	35	
tM	CEx valid to HIOE / HIOW	50	30	25	10	5	
tN	CEx hold	15	10	10	10	10	